

Compal Confidential

STORM2 M/B Schematic

LA-E292P

Rev: 0.3_B

2016.09.08

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	COVER PAGE
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				Custom	LA-E292P
				Date:	Thursday, September 08, 2016 Sheet 1 of 75

STORM 2 Block-Diagram

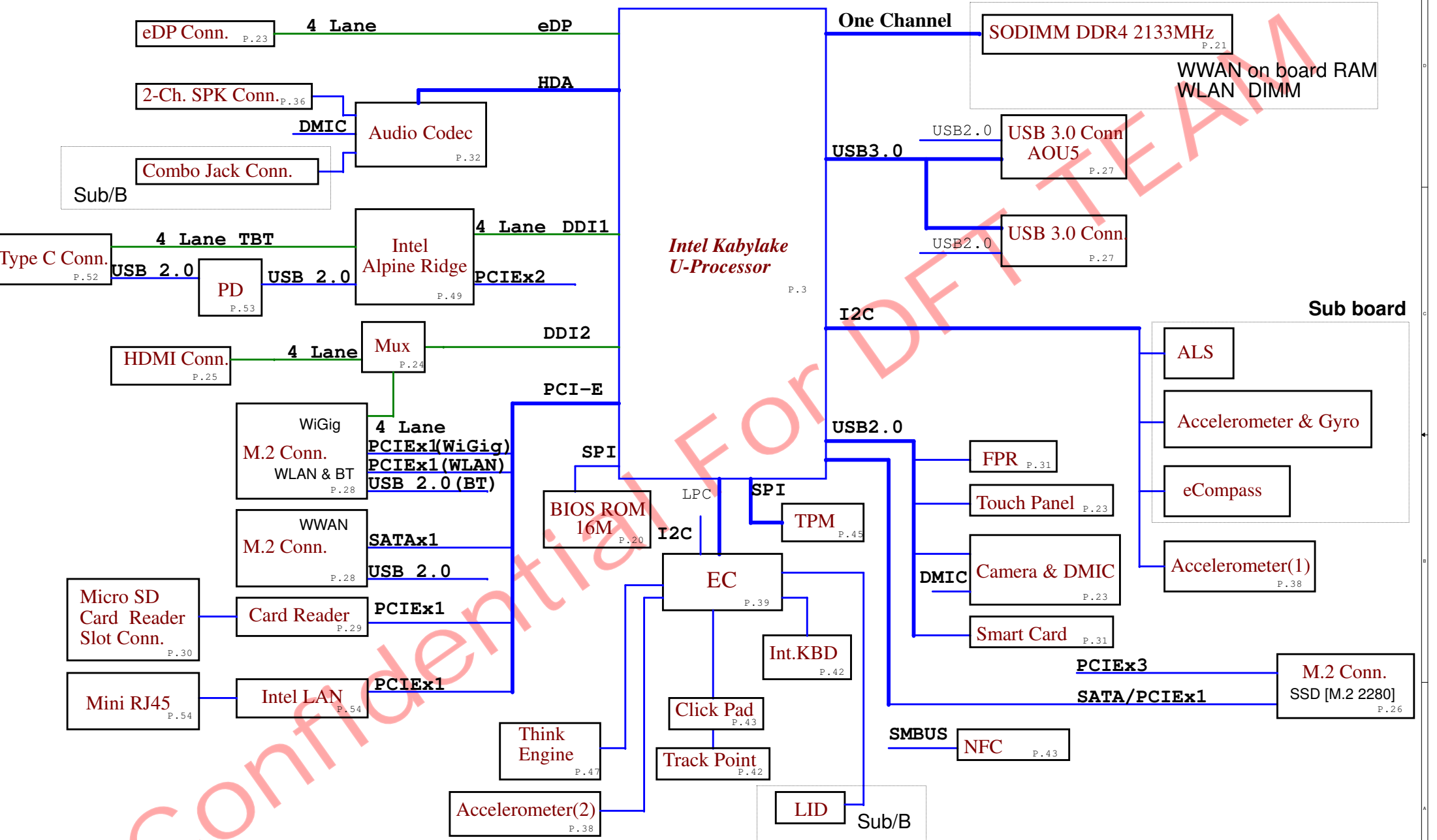


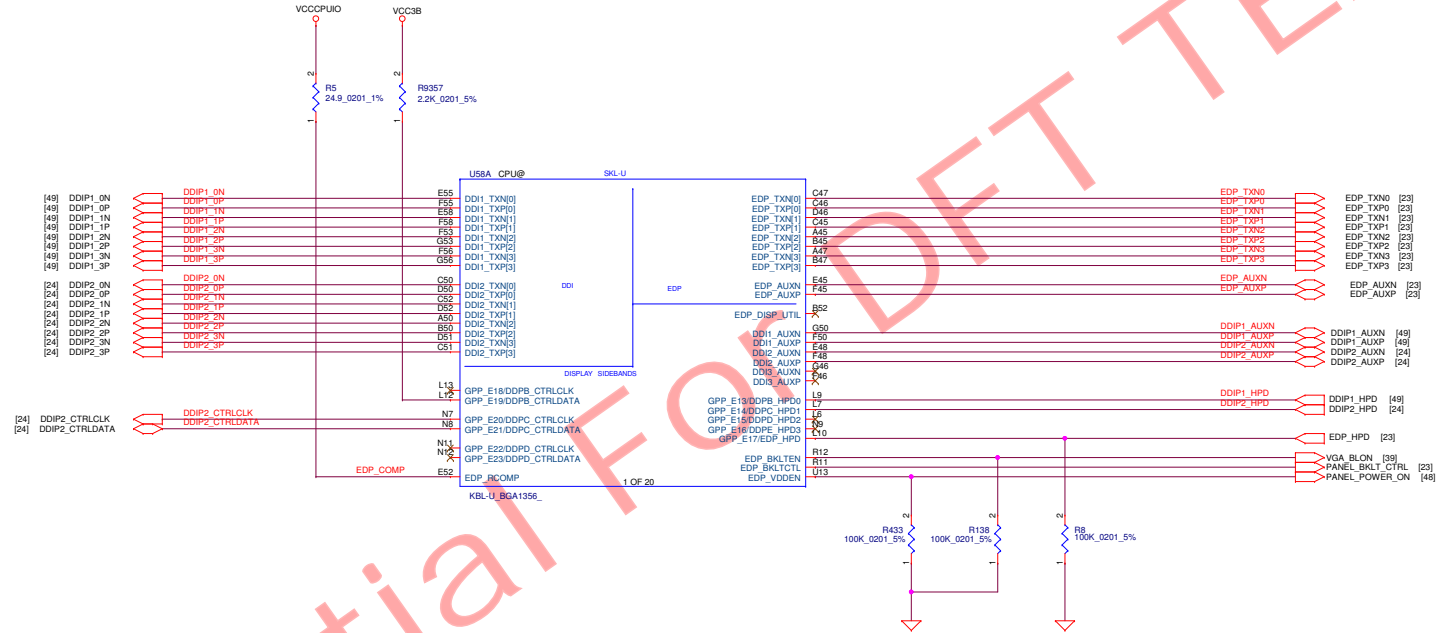
TABLE : Function Strap

DDPB_CTRLDATA

HIGH Port B is detected.
LOW Port B is not detected.

DDPC_CTRLDATA

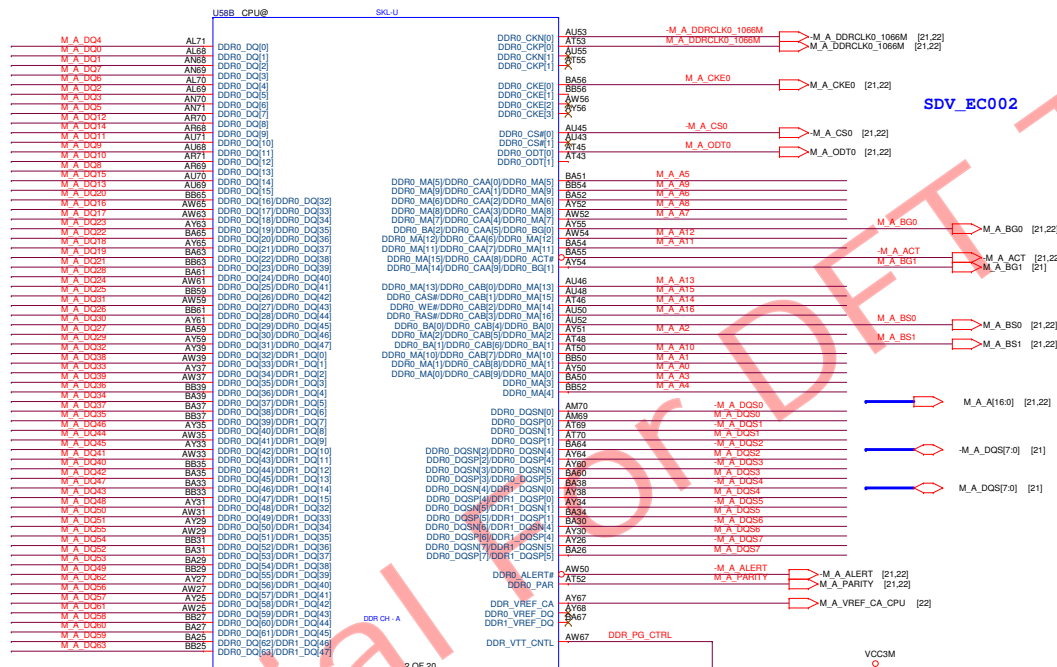
HIGH Port C is detected.
LOW Port C is not detected.



	Pin	Interleave	Non-Interleave
Block 0	AL71	DDRO_DQ[0]	DDRO_DQ[0]
	AL68	DDRO_DQ[1]	DDRO_DQ[1]
	AN68	DDRO_DQ[2]	DDRO_DQ[2]
	AN69	DDRO_DQ[3]	DDRO_DQ[3]
	AL70	DDRO_DQ[4]	DDRO_DQ[4]
	AL69	DDRO_DQ[5]	DDRO_DQ[5]
	AN70	DDRO_DQ[6]	DDRO_DQ[6]
	AN71	DDRO_DQ[7]	DDRO_DQ[7]
	AR70	DDRO_DQ[8]	DDRO_DQ[8]
	AR68	DDRO_DQ[9]	DDRO_DQ[9]
	AU71	DDRO_DQ[10]	DDRO_DQ[10]
	AU68	DDRO_DQ[11]	DDRO_DQ[11]
	AR71	DDRO_DQ[12]	DDRO_DQ[12]
	AR69	DDRO_DQ[13]	DDRO_DQ[13]
	AU70	DDRO_DQ[14]	DDRO_DQ[14]
	AU69	DDRO_DQ[15]	DDRO_DQ[15]
Block 3	BB65	DDRO_DQ[32]	DDRO_DQ[32]
	AW65	DDRO_DQ[33]	DDRO_DQ[33]
	AW63	DDRO_DQ[34]	DDRO_DQ[34]
	AY63	DDRO_DQ[35]	DDRO_DQ[35]
	BA65	DDRO_DQ[36]	DDRO_DQ[36]
	AY65	DDRO_DQ[37]	DDRO_DQ[37]
	BA63	DDRO_DQ[38]	DDRO_DQ[38]
	BB63	DDRO_DQ[39]	DDRO_DQ[39]
	BA61	DDRO_DQ[40]	DDRO_DQ[40]
	AW64	DDRO_DQ[41]	DDRO_DQ[41]
	BB59	DDRO_DQ[42]	DDRO_DQ[42]
	AW59	DDRO_DQ[43]	DDRO_DQ[43]
	BB61	DDRO_DQ[44]	DDRO_DQ[44]
	AR71	DDRO_DQ[45]	DDRO_DQ[45]
	BA59	DDRO_DQ[46]	DDRO_DQ[46]
	AY59	DDRO_DQ[47]	DDRO_DQ[47]
Block 4	AY39	DDRO_DQ[48]	DDRI_DQ[0]
	AW39	DDRO_DQ[33]	DDRI_DQ[1]
	AY37	DDRO_DQ[34]	DDRI_DQ[2]
	AW37	DDRO_DQ[35]	DDRI_DQ[3]
	BB39	DDRO_DQ[36]	DDRI_DQ[4]
	BA39	DDRO_DQ[37]	DDRI_DQ[5]
	BA37	DDRO_DQ[38]	DDRI_DQ[6]
	BB37	DDRO_DQ[39]	DDRI_DQ[7]
	AY35	DDRO_DQ[40]	DDRI_DQ[8]
	AW35	DDRO_DQ[41]	DDRI_DQ[9]
	AY33	DDRO_DQ[42]	DDRI_DQ[10]
	AW33	DDRO_DQ[43]	DDRI_DQ[11]
	BB35	DDRO_DQ[44]	DDRI_DQ[12]
	BA35	DDRO_DQ[45]	DDRI_DQ[13]
	BA33	DDRO_DQ[46]	DDRI_DQ[14]
	BB33	DDRO_DQ[47]	DDRI_DQ[15]
Block 6	AY31	DDRO_DQ[48]	DDRI_DQ[32]
	AW31	DDRO_DQ[49]	DDRI_DQ[33]
	AY29	DDRO_DQ[50]	DDRI_DQ[34]
	AW29	DDRO_DQ[51]	DDRI_DQ[35]
	BB31	DDRO_DQ[52]	DDRI_DQ[36]
	BA31	DDRO_DQ[53]	DDRI_DQ[37]
	BA29	DDRO_DQ[54]	DDRI_DQ[38]
	AY27	DDRO_DQ[55]	DDRI_DQ[39]
	AW27	DDRO_DQ[56]	DDRI_DQ[40]
	AW27	DDRO_DQ[57]	DDRI_DQ[41]
	AY25	DDRO_DQ[58]	DDRI_DQ[42]
	AW25	DDRO_DQ[59]	DDRI_DQ[43]
	BB27	DDRO_DQ[60]	DDRI_DQ[44]
	BA25	DDRO_DQ[61]	DDRI_DQ[45]
	BA25	DDRO_DQ[62]	DDRI_DQ[46]
	BB25	DDRO_DQ[63]	DDRI_DQ[47]

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDRO_DQ[0]	DDRO_DQ[0]
	AL68	DDRO_DQ[1]	DDRO_DQ[1]
	AN68	DDRO_DQ[2]	DDRO_DQ[2]
	AN69	DDRO_DQ[3]	DDRO_DQ[3]
	AL70	DDRO_DQ[4]	DDRO_DQ[4]
	AL69	DDRO_DQ[5]	DDRO_DQ[5]
	AN70	DDRO_DQ[6]	DDRO_DQ[6]
	AN71	DDRO_DQ[7]	DDRO_DQ[7]
	AR70	DDRO_DQ[8]	DDRO_DQ[8]
	AR68	DDRO_DQ[9]	DDRO_DQ[9]
	AU71	DDRO_DQ[10]	DDRO_DQ[10]
	AU68	DDRO_DQ[11]	DDRO_DQ[11]
	AR71	DDRO_DQ[12]	DDRO_DQ[12]
	AR69	DDRO_DQ[13]	DDRO_DQ[13]
AU70	DDRO_DQ[14]	DDRO_DQ[14]	
AU69	DDRO_DQ[15]	DDRO_DQ[15]	
Block 2	BB65	DDRO_DQ[32]	DDRO_DQ[32]
	AW65	DDRO_DQ[33]	DDRO_DQ[33]
	AW63	DDRO_DQ[34]	DDRO_DQ[34]
	AY63	DDRO_DQ[35]	DDRO_DQ[35]
	BA65	DDRO_DQ[36]	DDRO_DQ[36]
	AY65	DDRO_DQ[37]	DDRO_DQ[37]
	BA63	DDRO_DQ[38]	DDRO_DQ[38]
	BB63	DDRO_DQ[39]	DDRO_DQ[39]
	BA61	DDRO_DQ[40]	DDRO_DQ[40]
	AW64	DDRO_DQ[41]	DDRO_DQ[41]
	BB59	DDRO_DQ[42]	DDRO_DQ[42]
	AW59	DDRO_DQ[43]	DDRO_DQ[43]
	BB61	DDRO_DQ[44]	DDRO_DQ[44]
	AR71	DDRO_DQ[45]	DDRO_DQ[45]
BA59	DDRO_DQ[46]	DDRO_DQ[46]	
AY59	DDRO_DQ[47]	DDRO_DQ[47]	
Block 4	AY39	DDRO_DQ[48]	DDRI_DQ[0]
	AW39	DDRO_DQ[33]	DDRI_DQ[1]
	AY37	DDRO_DQ[34]	DDRI_DQ[2]
	AW37	DDRO_DQ[35]	DDRI_DQ[3]
	BB39	DDRO_DQ[36]	DDRI_DQ[4]
	BA39	DDRO_DQ[37]	DDRI_DQ[5]
	BA37	DDRO_DQ[38]	DDRI_DQ[6]
	BB37	DDRO_DQ[39]	DDRI_DQ[7]
	AY35	DDRO_DQ[40]	DDRI_DQ[8]
	AW35	DDRO_DQ[41]	DDRI_DQ[9]
	AY33	DDRO_DQ[42]	DDRI_DQ[10]
	AW33	DDRO_DQ[43]	DDRI_DQ[11]
	BB35	DDRO_DQ[44]	DDRI_DQ[12]
	BA35	DDRO_DQ[45]	DDRI_DQ[13]
BA33	DDRO_DQ[46]	DDRI_DQ[14]	
BB33	DDRO_DQ[47]	DDRI_DQ[15]	
Block 6	AY31	DDRO_DQ[48]	DDRI_DQ[32]
	AW31	DDRO_DQ[49]	DDRI_DQ[33]
	AY29	DDRO_DQ[50]	DDRI_DQ[34]
	AW29	DDRO_DQ[51]	DDRI_DQ[35]
	BB31	DDRO_DQ[52]	DDRI_DQ[36]
	BA31	DDRO_DQ[53]	DDRI_DQ[37]
	BA29	DDRO_DQ[54]	DDRI_DQ[38]
	AY27	DDRO_DQ[55]	DDRI_DQ[39]
	AW27	DDRO_DQ[56]	DDRI_DQ[40]
	AW27	DDRO_DQ[57]	DDRI_DQ[41]
	AY25	DDRO_DQ[58]	DDRI_DQ[42]
	AW25	DDRO_DQ[59]	DDRI_DQ[43]
	BB27	DDRO_DQ[60]	DDRI_DQ[44]
	BA25	DDRO_DQ[61]	DDRI_DQ[45]
BB25	DDRO_DQ[62]	DDRI_DQ[46]	
		DDRI_DQ[47]	

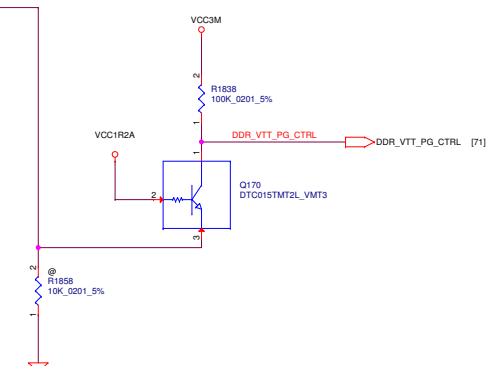
LOGIC



	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC



Pin	DDR3L	LPDDR3	DDR4
BA51	DDRO_MA[5]	DDRO_CAA[0]	DDRO_MA[5]
BB54	DDRO_MA[9]	DDRO_CAA[1]	DDRO_MA[9]
BA52	DDRO_MA[6]	DDRO_CAA[2]	DDRO_MA[6]
AY52	DDRO_MA[8]	DDRO_CAA[3]	DDRO_MA[8]
AW52	DDRO_MA[7]	DDRO_CAA[4]	DDRO_MA[7]
AY55	DDRO_BA[2]	DDRO_CAA[5]	DDRO_BG[0]
AW54	DDRO_MA[12]	DDRO_CAA[6]	DDRO_MA[12]
BT44	DDRO_MA[11]	DDRO_CAA[7]	DDRO_MA[11]
BA54	DDRO_MA[15]	DDRO_CAA[8]	DDRO_ACT#
AY54	DDRO_MA[14]	DDRO_CAA[9]	DDRO_BG[1]
AU46	DDRO_MA[13]	DDRO_CAB[0]	DDRO_MA[13]
AU48	DDRO_CASH	DDRO_CAB[1]	DDRO_MA[15]
AT46	DDRO_BA[2]	DDRO_CAB[2]	DDRO_MA[14]
AU50	DDRO_RAS#	DDRO_CAB[3]	DDRO_MA[16]
AU52	DDRO_BA[0]	DDRO_CAB[4]	DDRO_BA[0]
AY51	DDRO_MA[2]	DDRO_CAB[5]	DDRO_MA[2]
AT48	DDRO_BA[1]	DDRO_CAB[6]	DDRO_BA[1]
AT50	DDRO_MA[10]	DDRO_CAB[7]	DDRO_MA[10]
BB50	DDRO_MA[1]	DDRO_CAB[8]	DDRO_MA[1]
AY50	DDRO_MA[0]	DDRO_CAB[9]	DDRO_MA[0]
BA50	DDRO_MA[3]	Not Used	DDRO_MA[3]
BB52	DDRO_MA[4]	Not Used	DDRO_MA[4]

Pin	DDR3L	LPDDR3	DDR4
BA51	DDRO_MA[5]	DDRO_CAA[0]	DDRO_MA[5]
BB54	DDRO_MA[9]	DDRO_CAA[1]	DDRO_MA[9]
BA52	DDRO_MA[6]	DDRO_CAA[2]	DDRO_MA[6]
AY52	DDRO_MA[8]	DDRO_CAA[3]	DDRO_MA[8]
AW52	DDRO_MA[7]	DDRO_CAA[4]	DDRO_MA[7]
AY55	DDRO_BA[2]	DDRO_CAA[5]	DDRO_BG[0]
AW54	DDRO_MA[12]	DDRO_CAA[6]	DDRO_MA[12]
BT44	DDRO_MA[11]	DDRO_CAA[7]	DDRO_MA[11]
BA54	DDRO_MA[15]	DDRO_CAA[8]	DDRO_ACT#
AY54	DDRO_MA[14]	DDRO_CAA[9]	DDRO_BG[1]
AU46	DDRO_MA[13]	DDRO_CAB[0]	DDRO_MA[13]
AU48	DDRO_CASH#	DDRO_CAB[1]	DDRO_MA[15]
AT46	DDRO_BA[2]	DDRO_CAB[5]	DDRO_BA[14]
AU50	DDRO_RAS#	DDRO_CAB[3]	DDRO_MA[16]
AU52	DDRO_BA[0]	DDRO_CAB[4]	DDRO_BA[0]
AY51	DDRO_MA[2]	DDRO_CAB[5]	DDRO_MA[2]
AT48	DDRO_BA[1]	DDRO_CAB[6]	DDRO_BA[1]
AT50	DDRO_MA[10]	DDRO_CAB[7]	DDRO_MA[10]
BB50	DDRO_MA[1]	DDRO_CAB[8]	DDRO_MA[1]
AY50	DDRO_MA[0]	DDRO_CAB[9]	DDRO_MA[0]
BA50	DDRO_MA[3]	Not Used	DDRO_MA[3]
BB52	DDRO_MA[4]	Not Used	DDRO_MA[4]

LOGIC

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

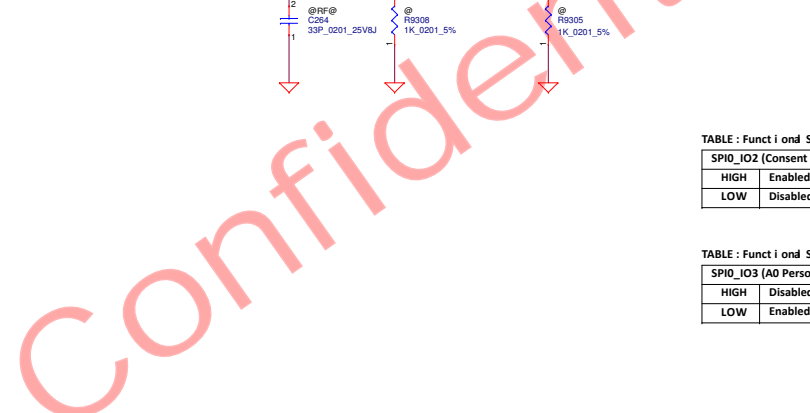
SPI0_MISO (JTAG ODT Diabler)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Conf i dent i d i t y)	
HIGH	Enable ME Crypto TLS with Conf i dent i d i t y
LOW	Disable ME Crypto TLS (Default)

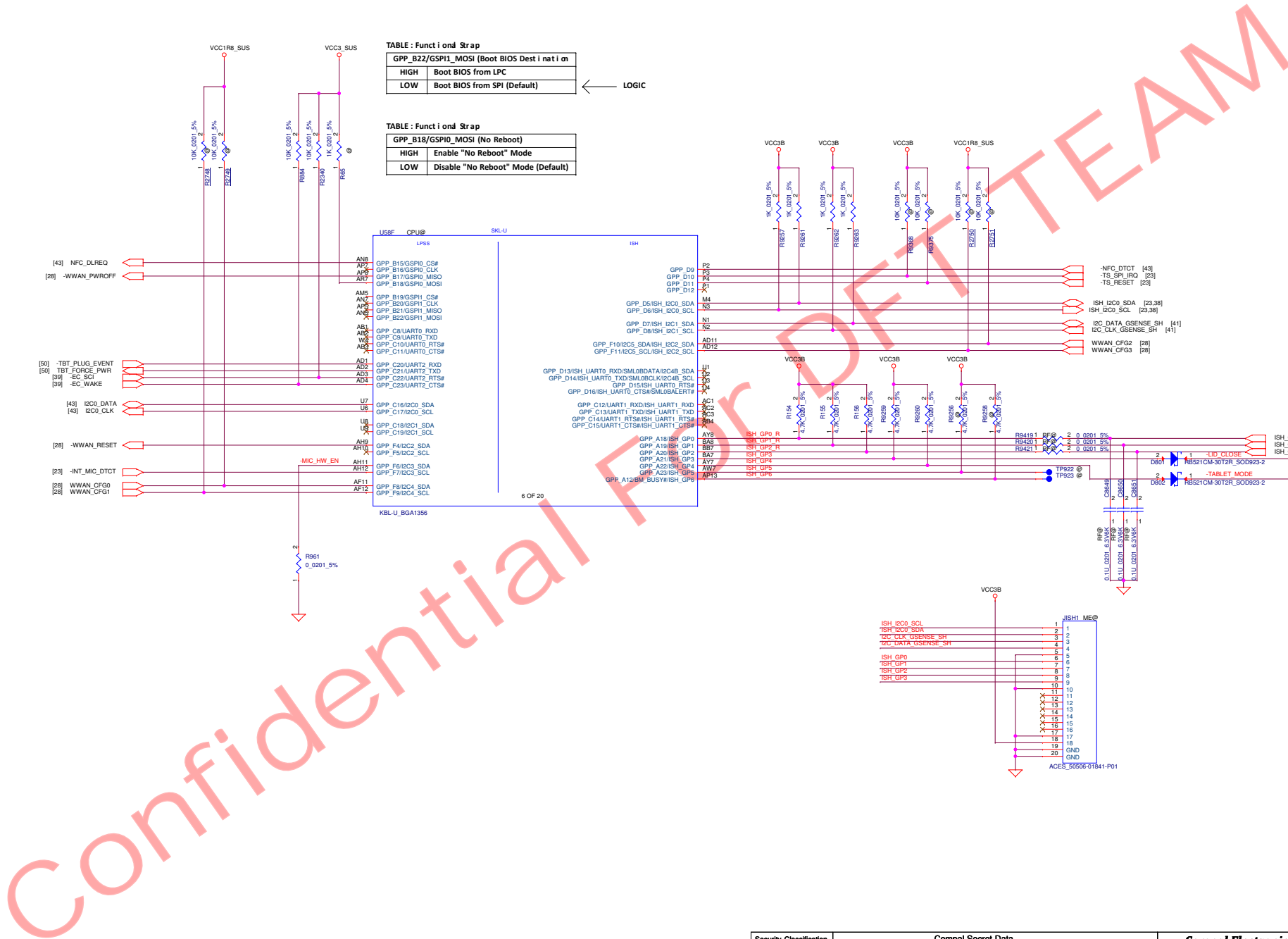
← LOGIC



SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

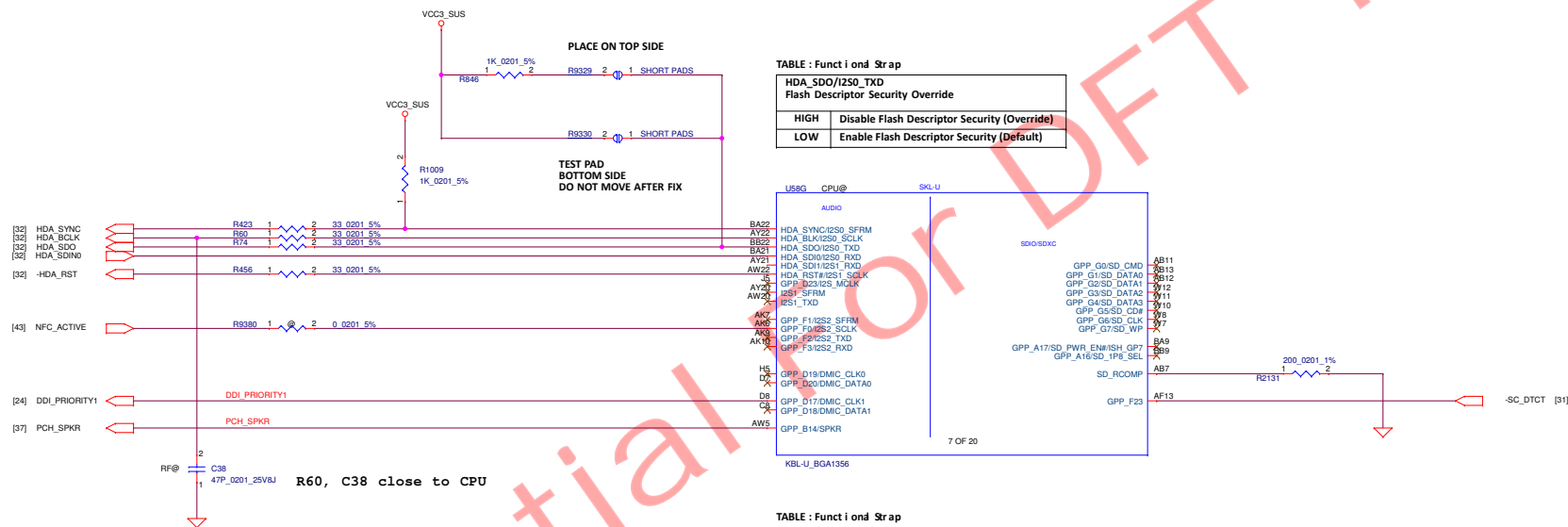
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	CPU(S116) : LPC/SPI/SMBUS/C-LINK	
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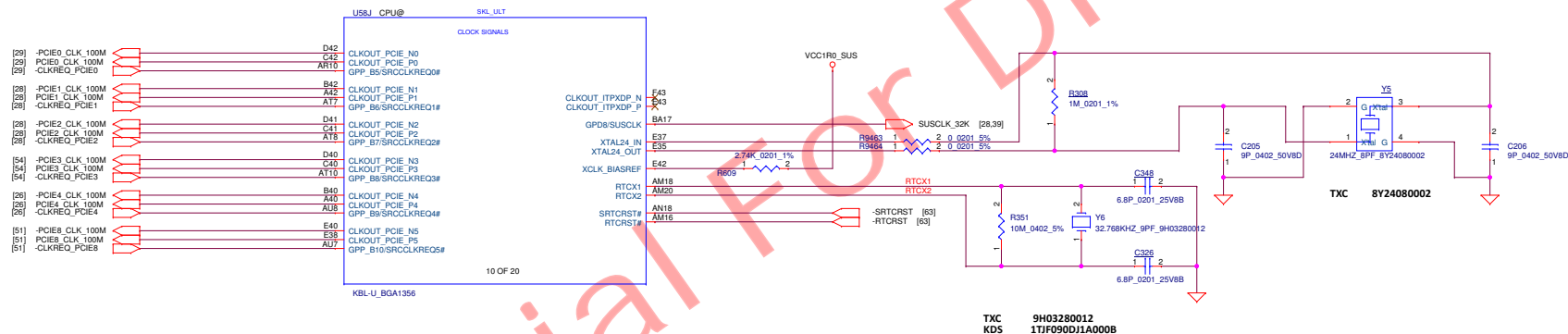


GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

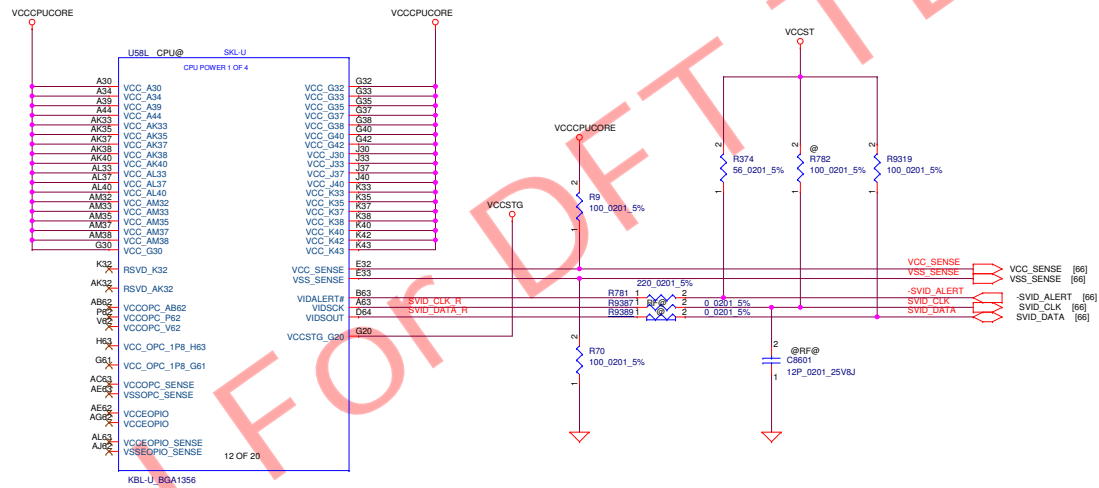
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	
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				Custom	LA-E29P2
				Date	Tuesday, September 08, 2016 10:56 AM
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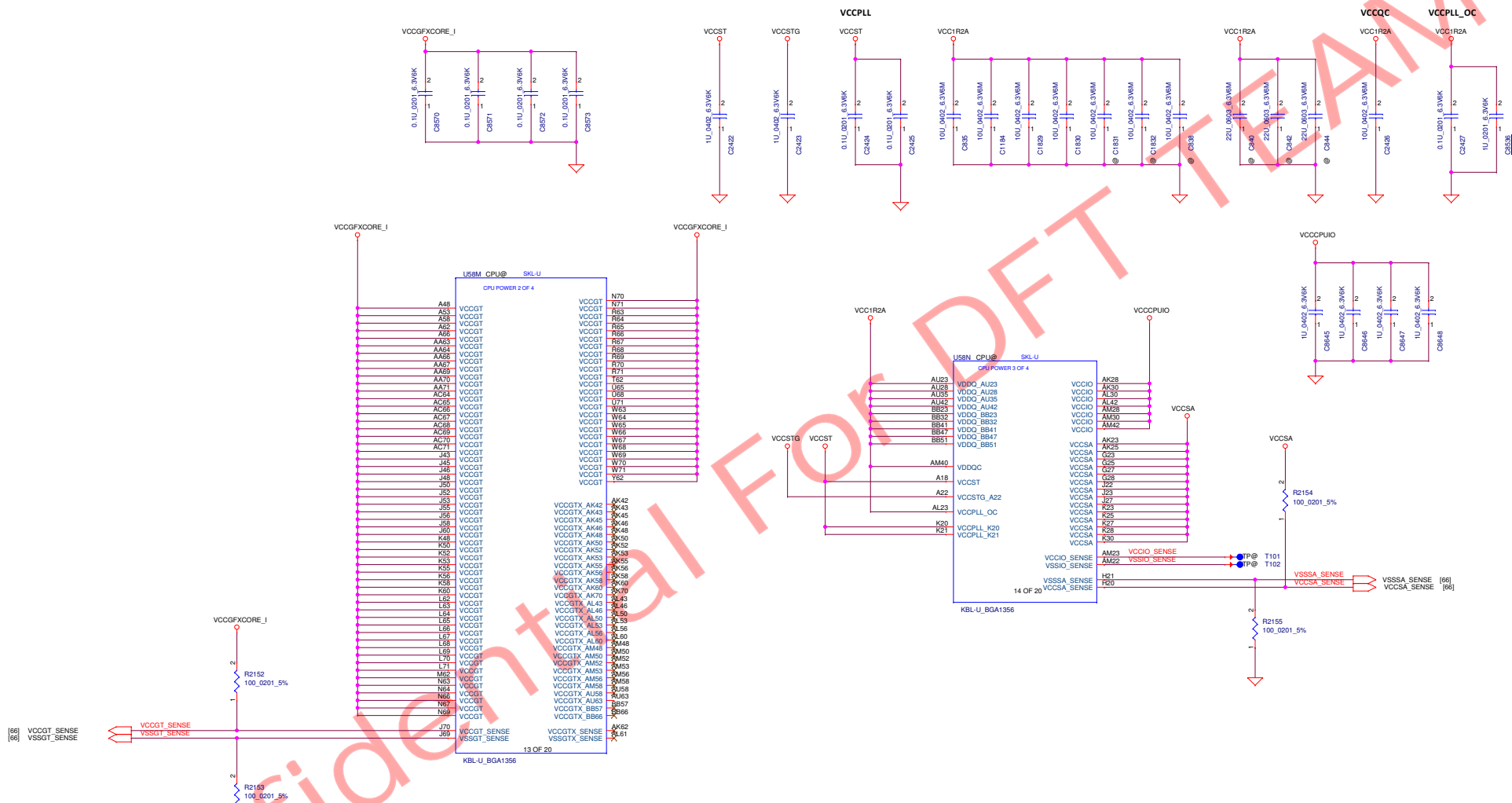


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Confidential For DFT TEAM

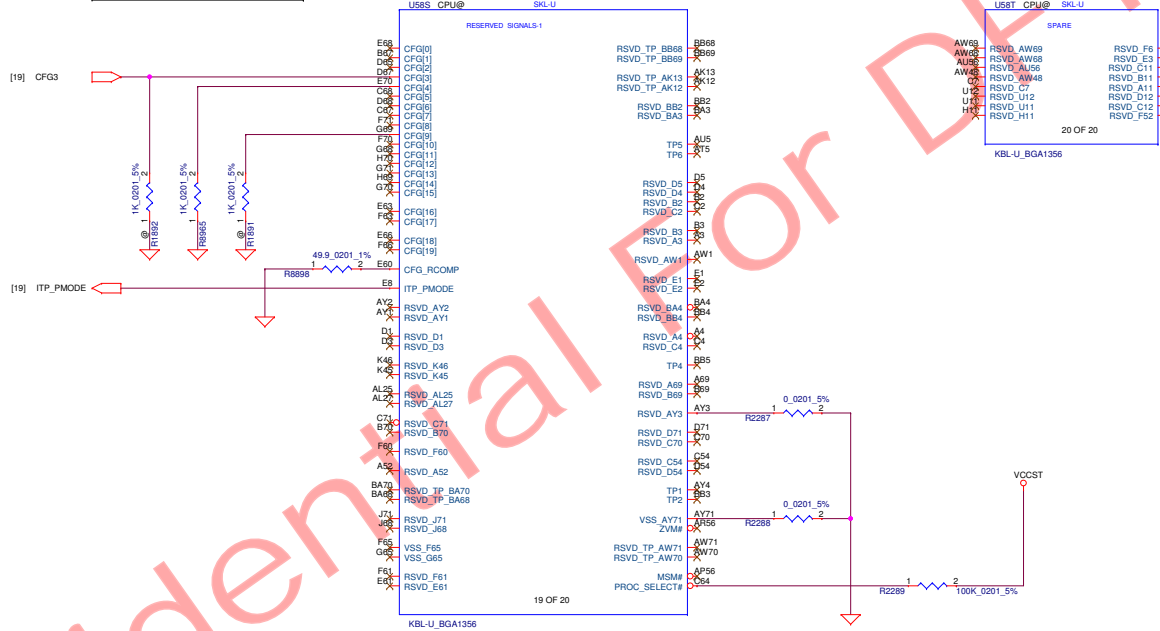


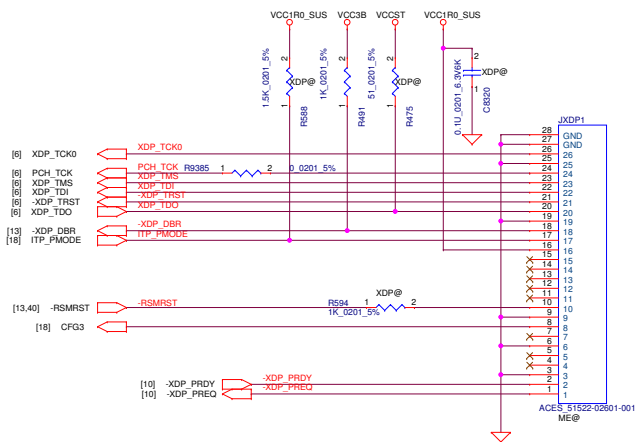
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TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-assert 1 : No Stall 0 : Stall
CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] set t in 0 : MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communicat i on 1 : Enabled 0 : Disabled





TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R2559	ASM	NO_ASM
Page 18	R1982	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

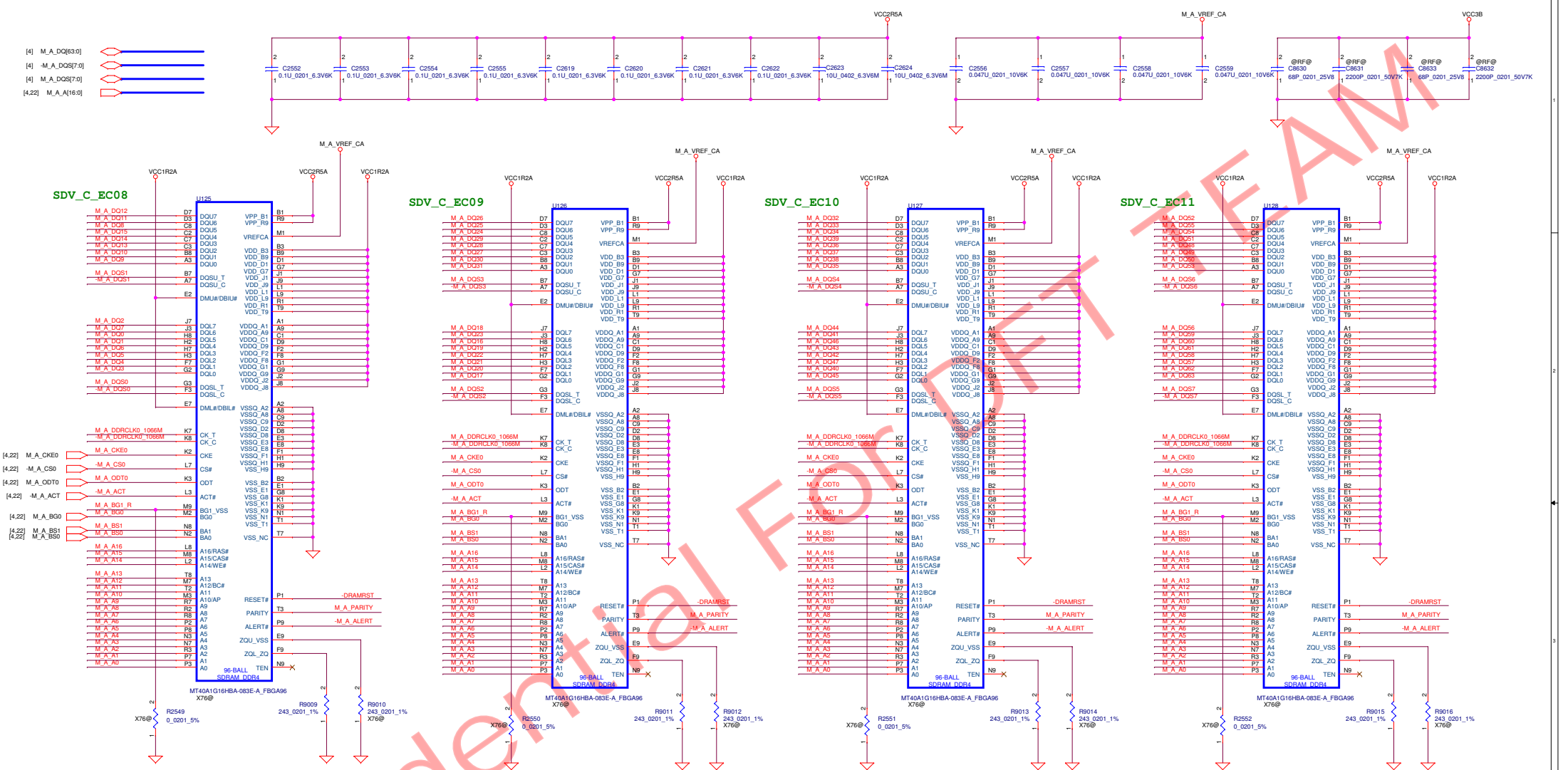
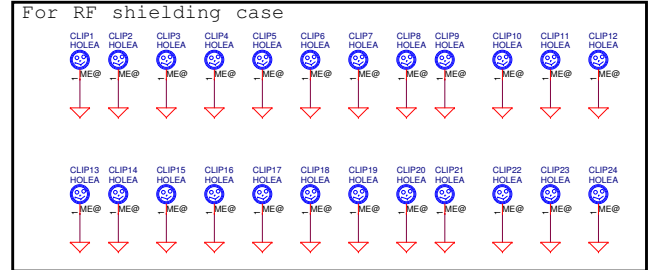
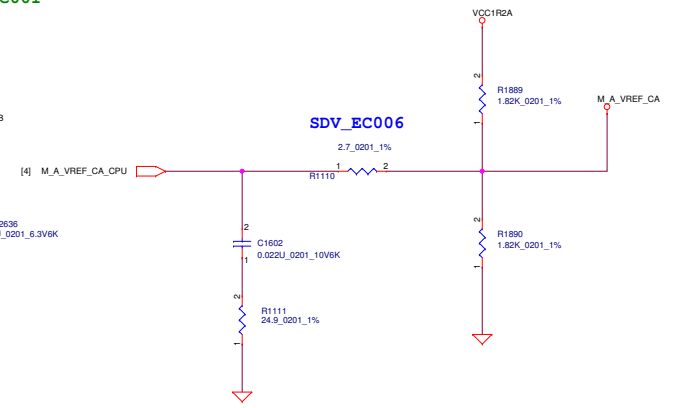
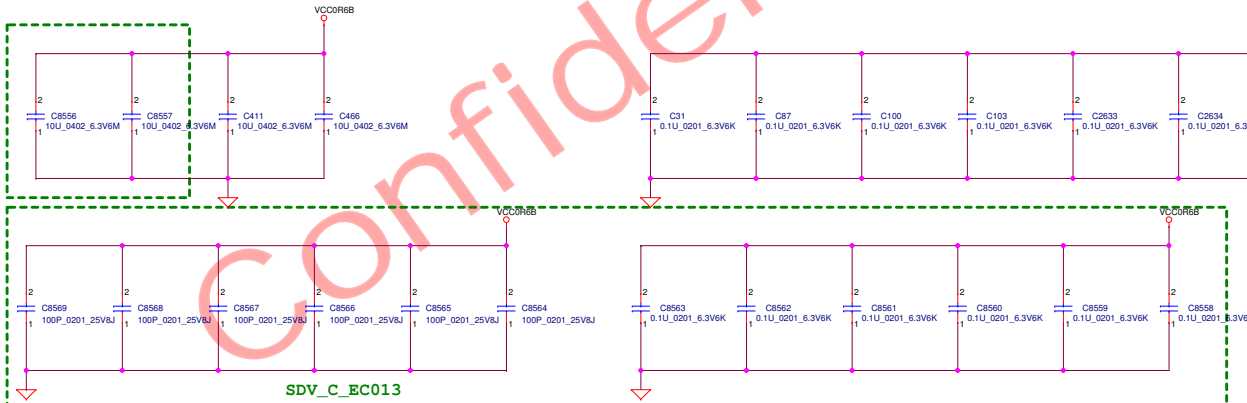
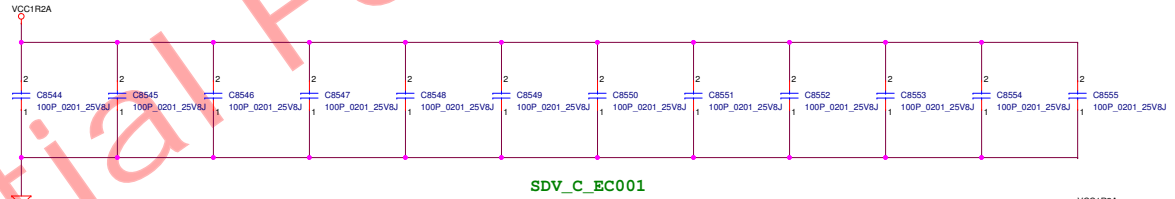
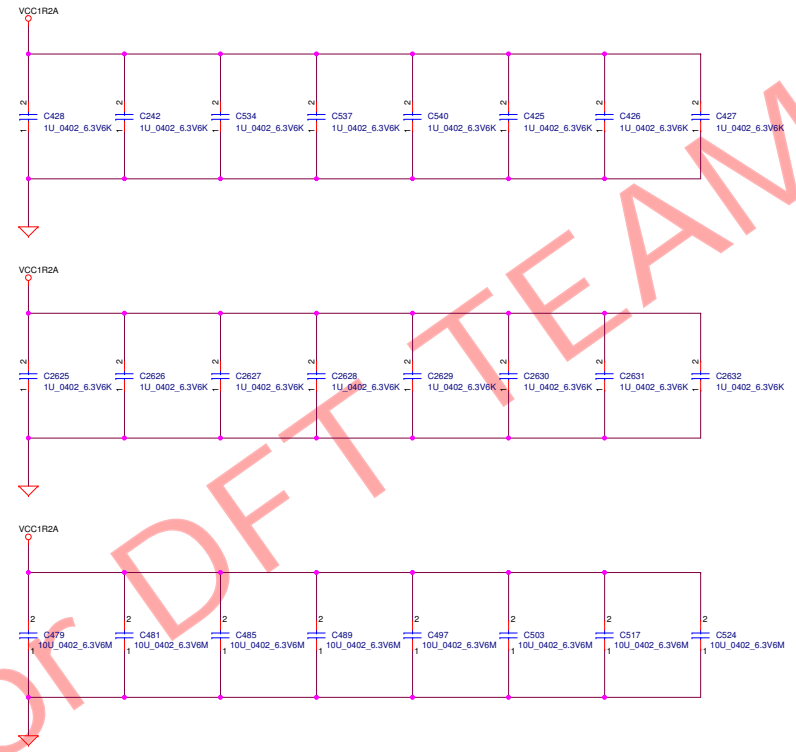
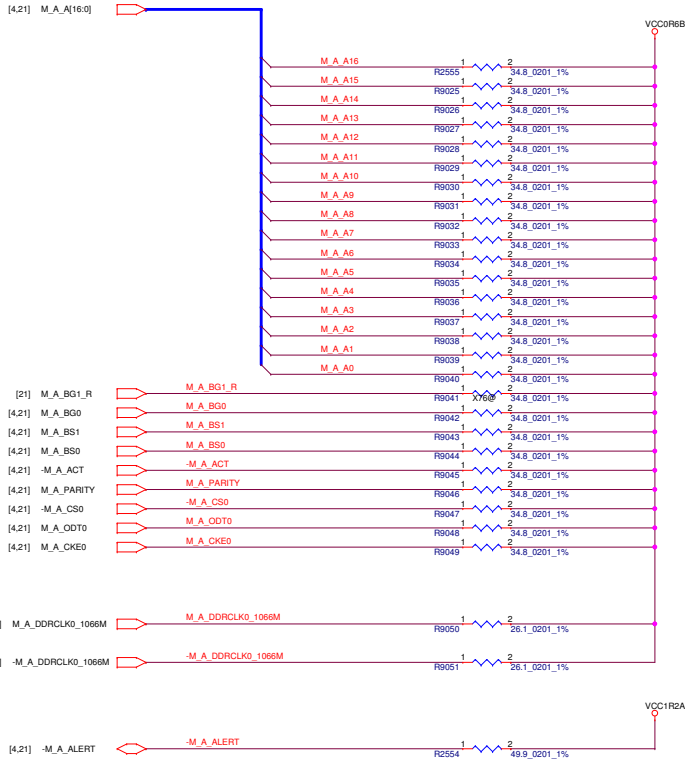


TABLE		
	SDP	DDP
[4.22] M_A_DDRCLK0_1066M [4.22] -M_A_DDRCLK0_1066M	ASM	NA
	ASM	NA
	ASM	NA
[4] M_A_BG1 [5] -DRAMRST	NA	ASM
	NA	ASM
[4.22] M_A_PARITY [4.22] -M_A_ALERT	0_5%	243_1%
	0_5%	243_1%
	0_5%	243_1%
	0_5%	243_1%





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				Customer	0.2
				Date	Thursday, September 08, 2016
				Sheet	22 of 102

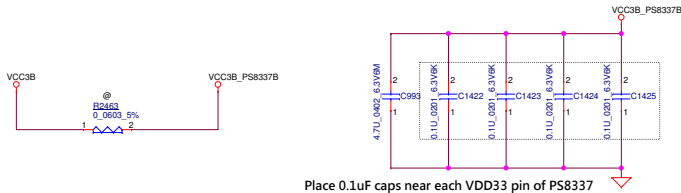
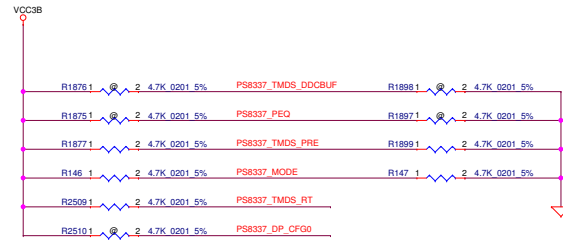


TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged
H TMDs Port has higher priority when both ports are plugged



TMDs DDCBUF (INT PD)	R1876	R1898
DDC Active Buffer	ASM	NO_ASM
DDC Pass Through w/ PU	ASM	ASM
DDC Pass Through w/o PU	NO_ASM	NO_ASM

LOGIC

PEQ (INT PD)	R1875	R1897
HEQ 15dB	ASM	NO_ASM
LLEQ 5dB	ASM	ASM
LEQ 12dB	NO_ASM	NO_ASM

LOGIC

TMDs PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

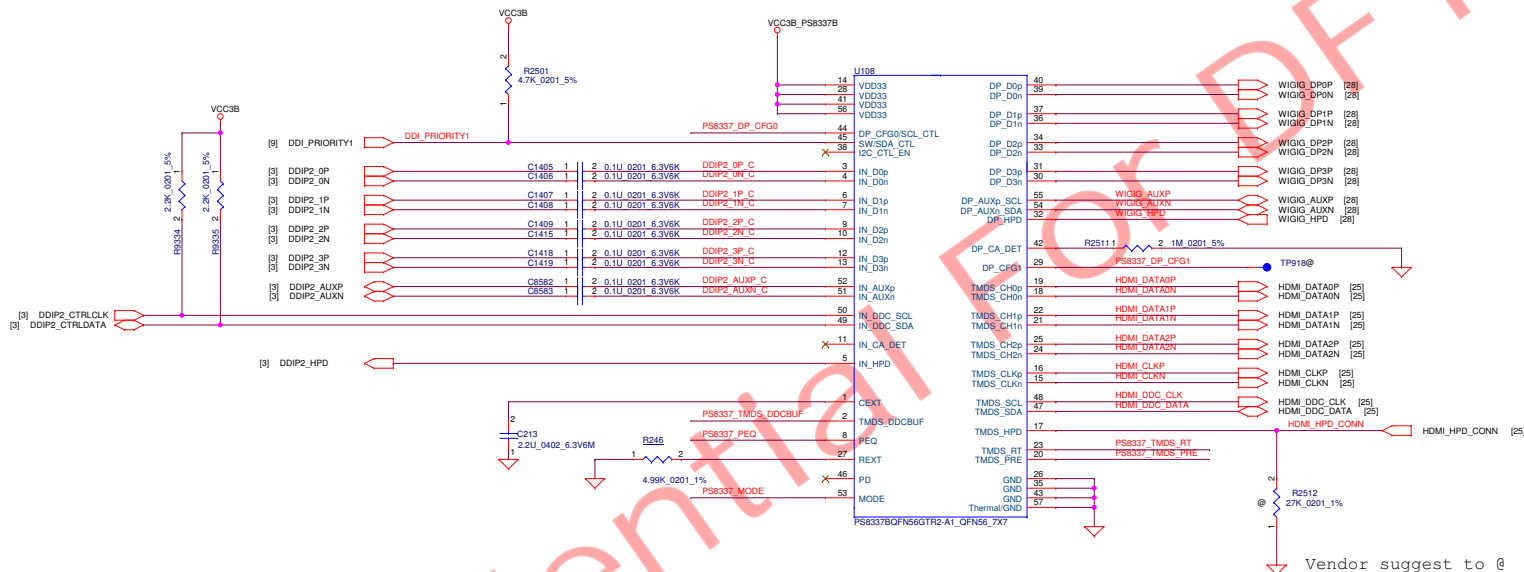
LOGIC

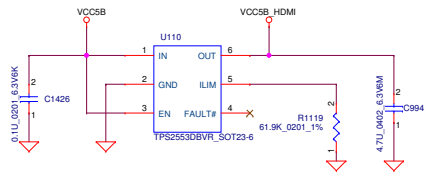
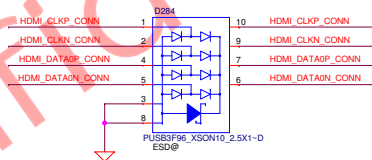
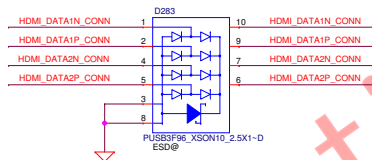
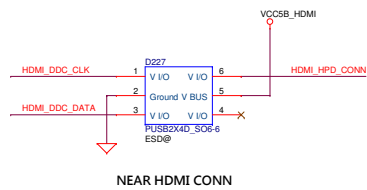
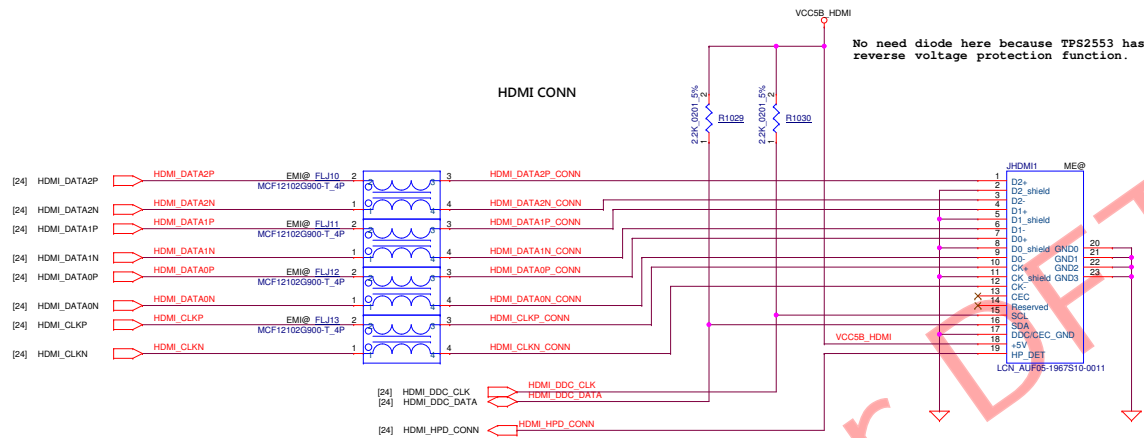
MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

LOGIC

TMDs RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

LOGIC



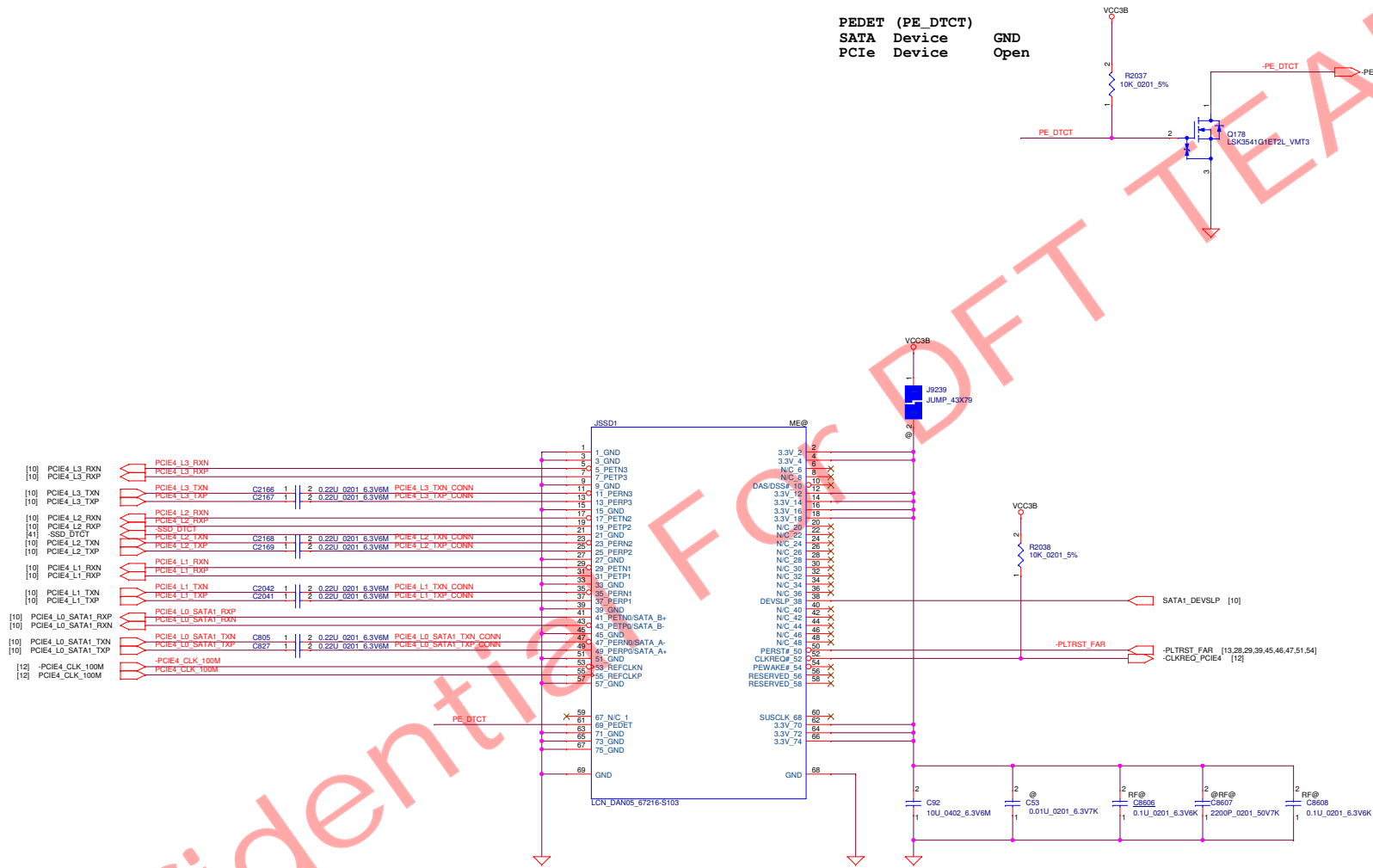


Current Limit Target : 400mA

Requirement : 300mA

HDMI Spec : 50mA - 500mA

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				Date	Thursday, September 08, 2016
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				Rev	0.3

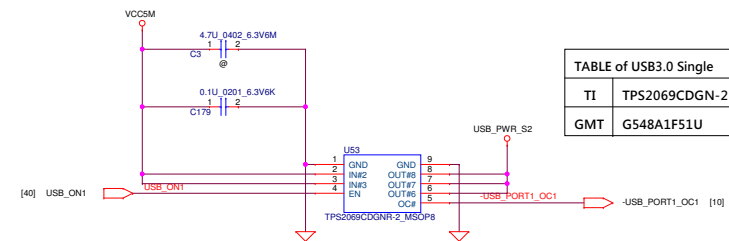
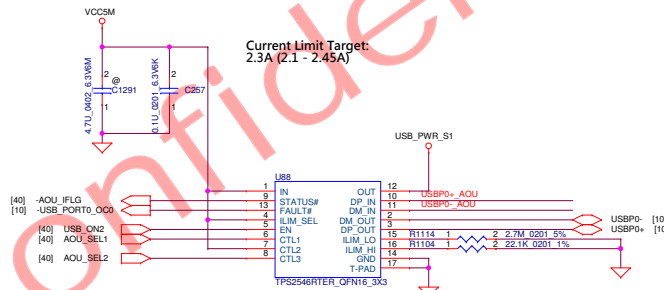
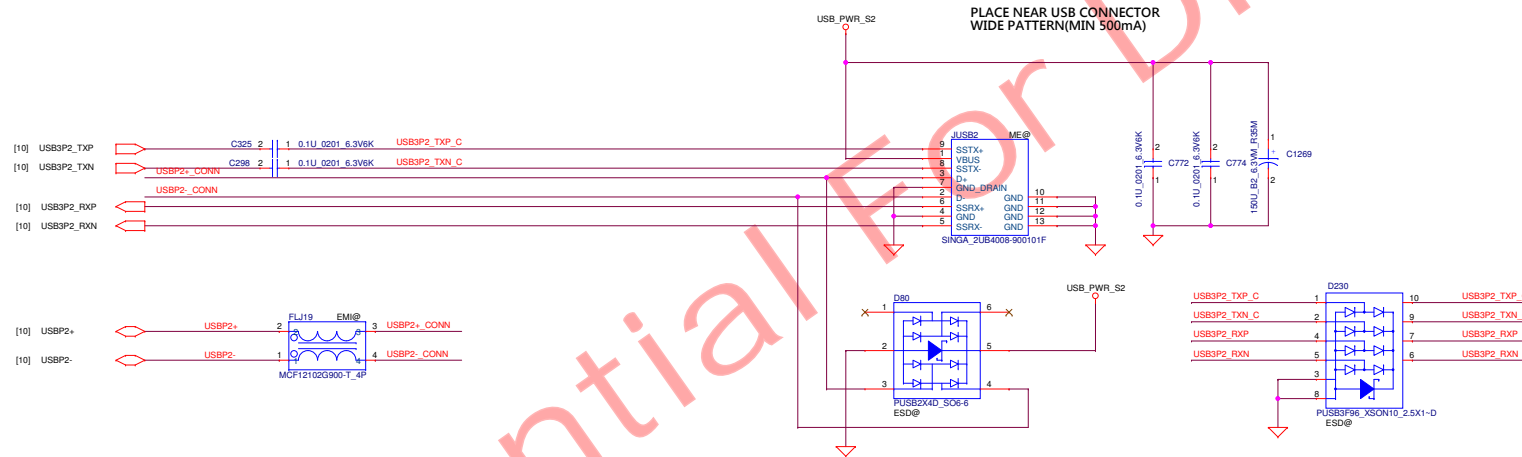
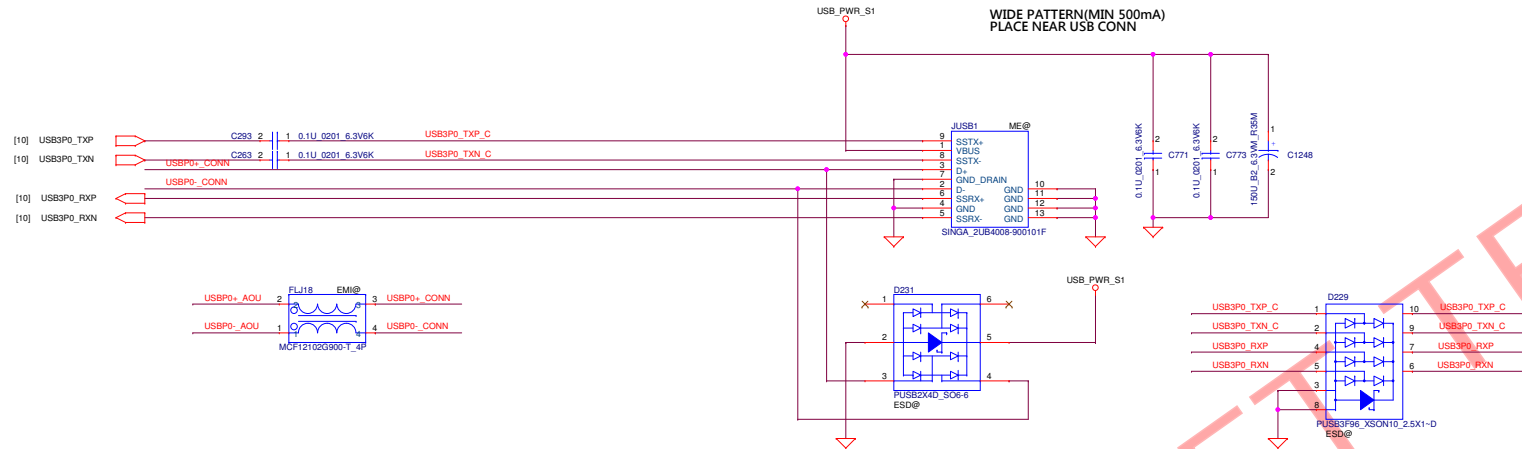


TABLE of USB3.0 Single		
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GMT	G548A1F51U	

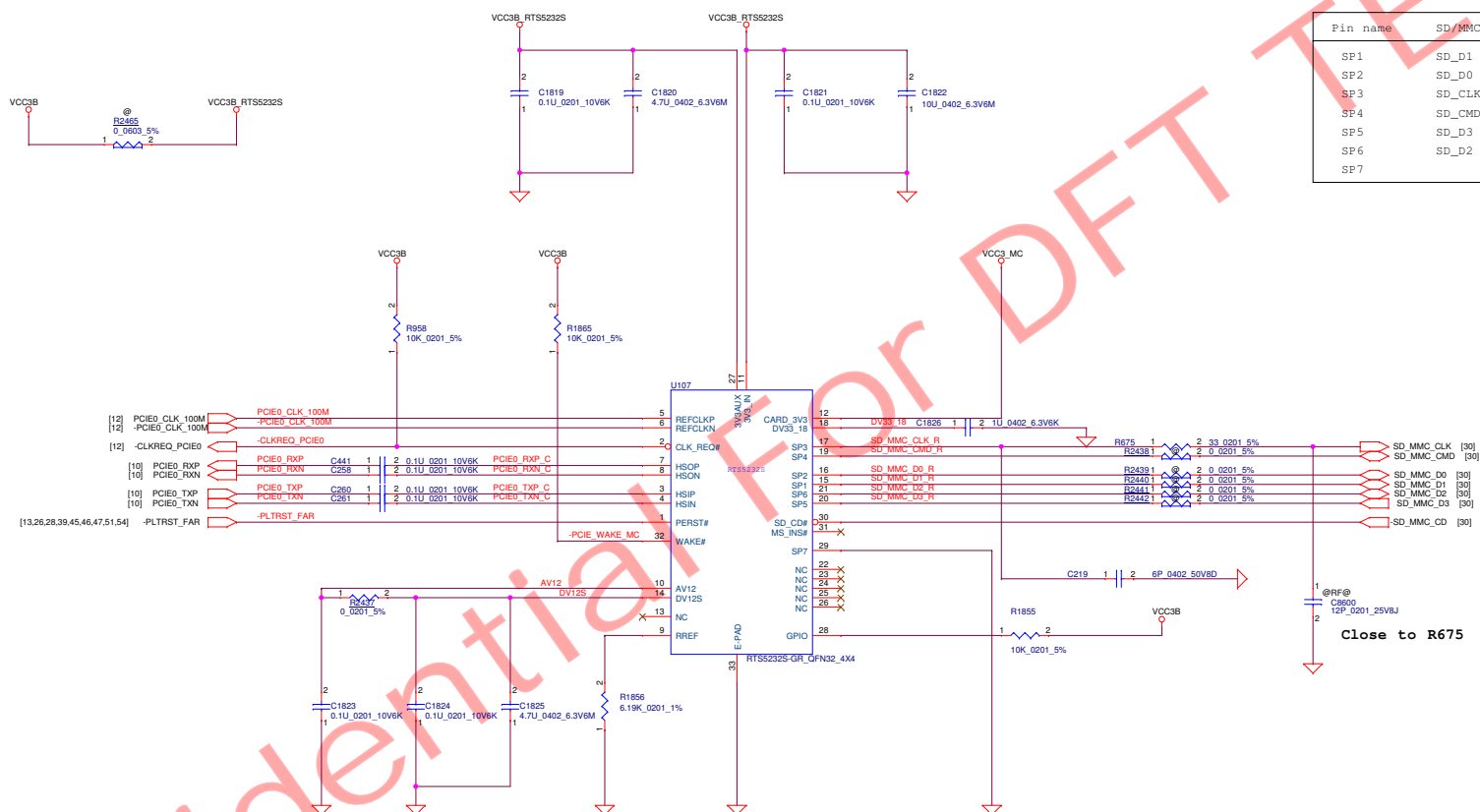
3042S3 CONNECTOR



2630S3 CONNECTOR



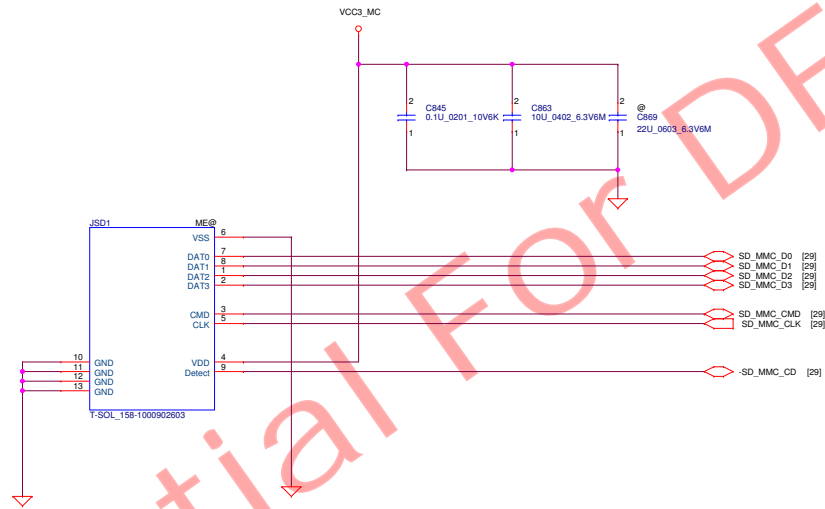
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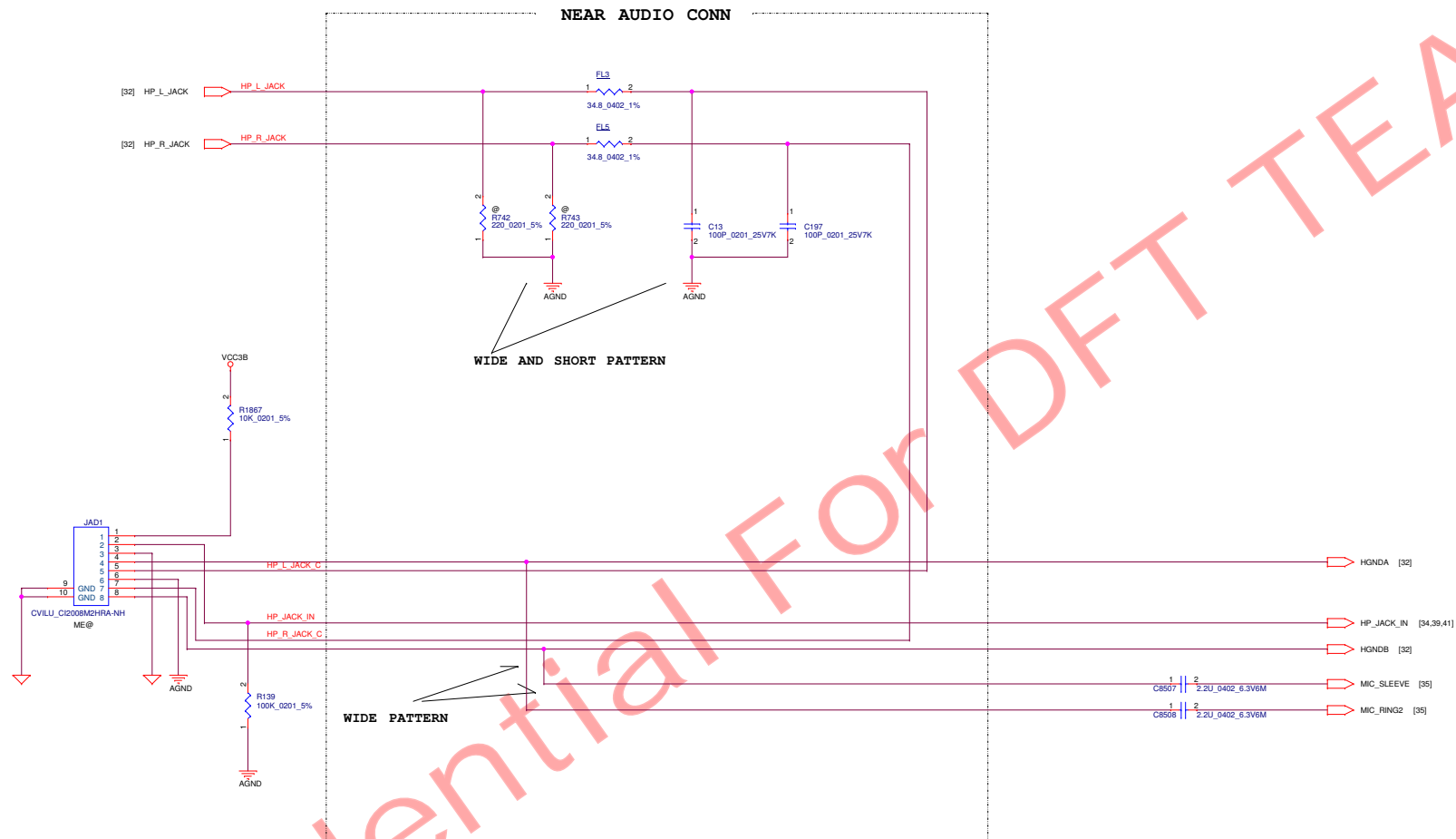
TABLE

Pin name	SD/MMC	MEMORSTICK
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		

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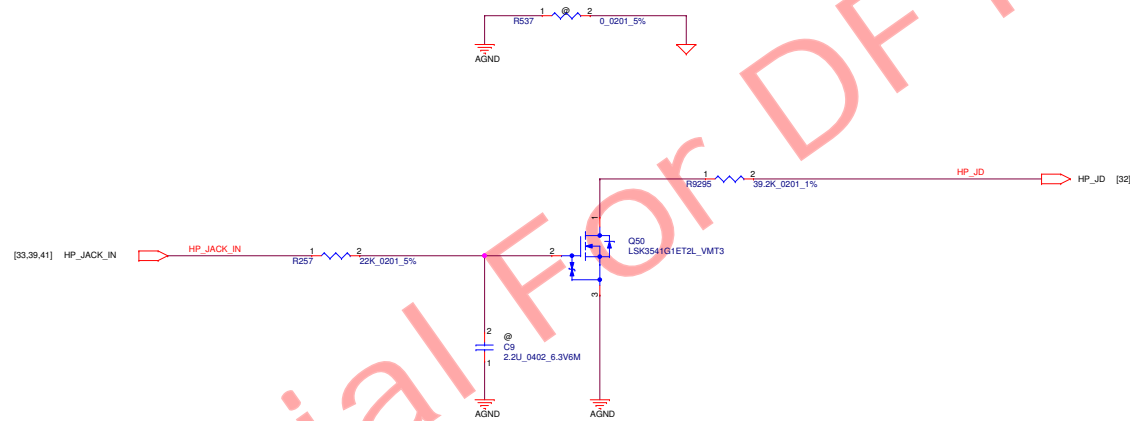


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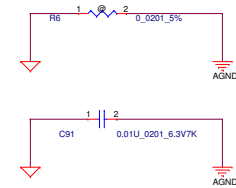
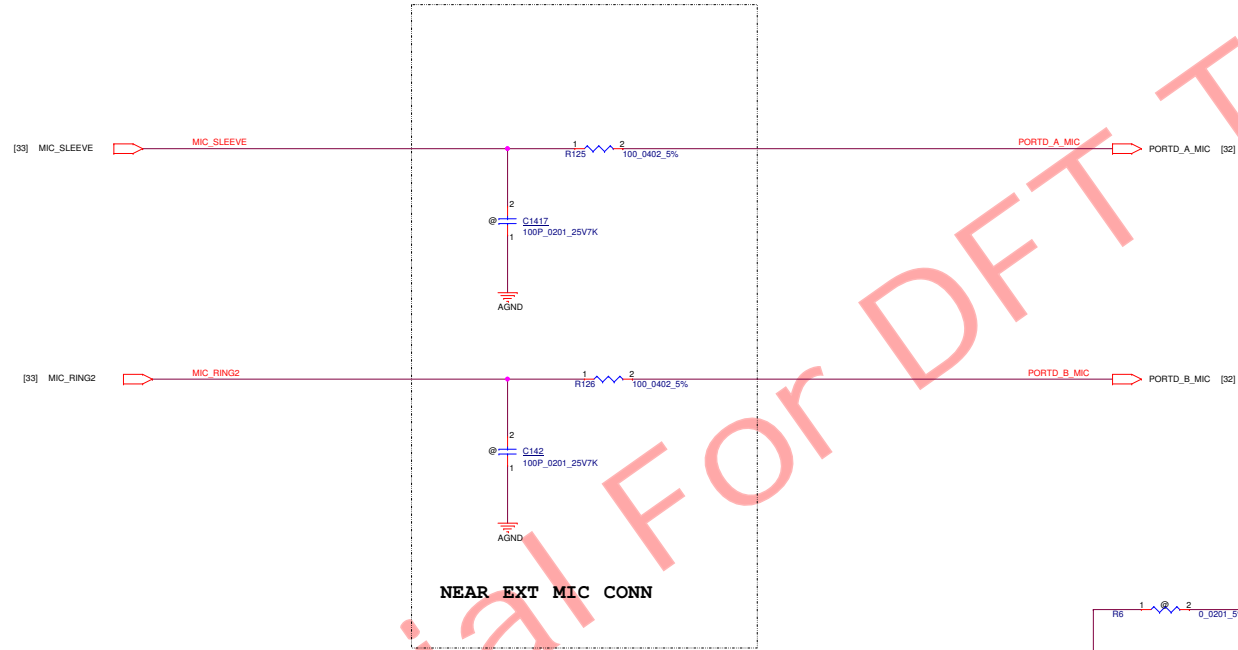


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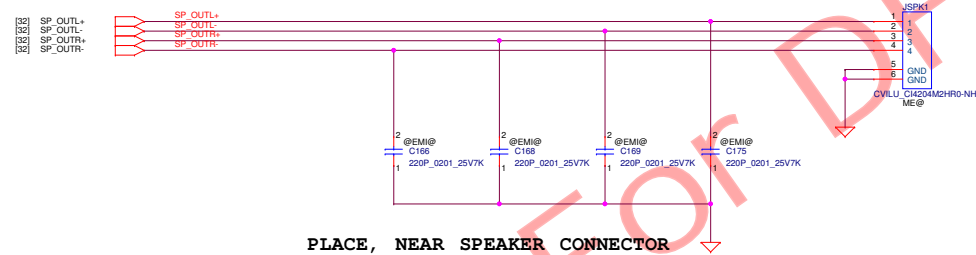
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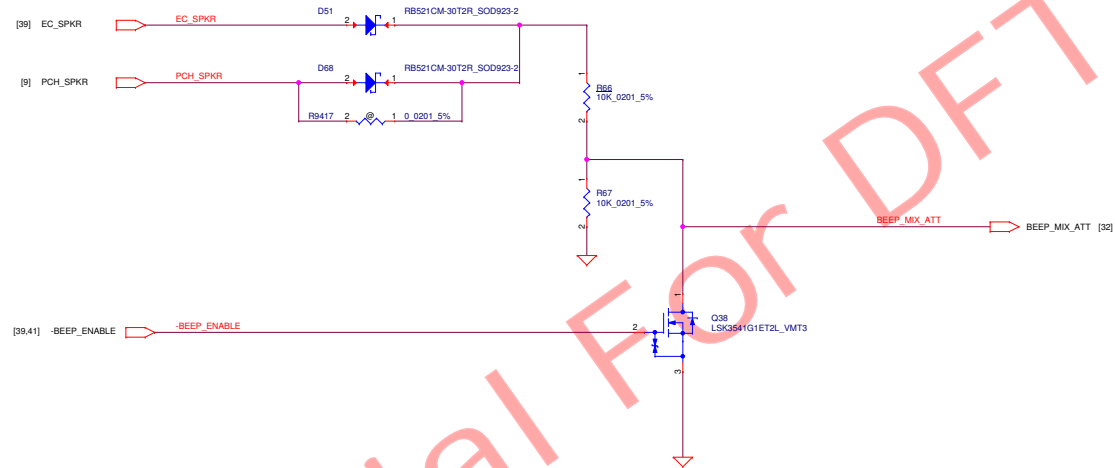
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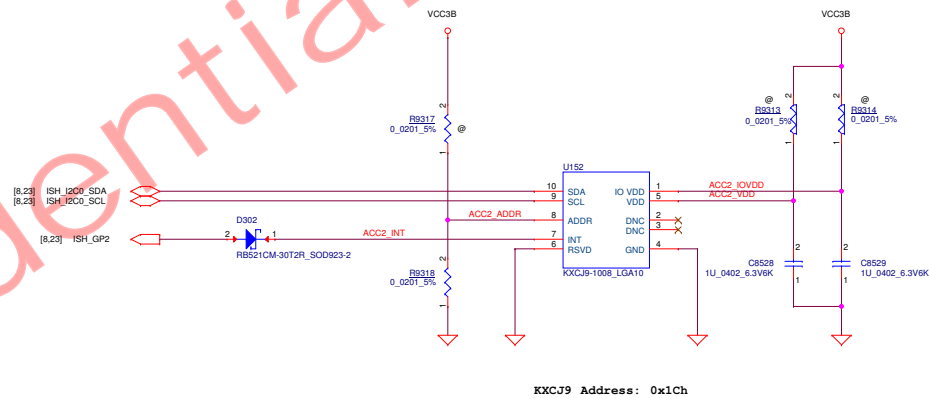
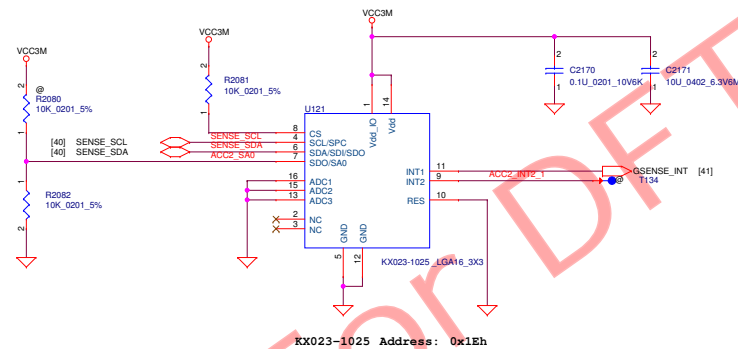
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TABLE

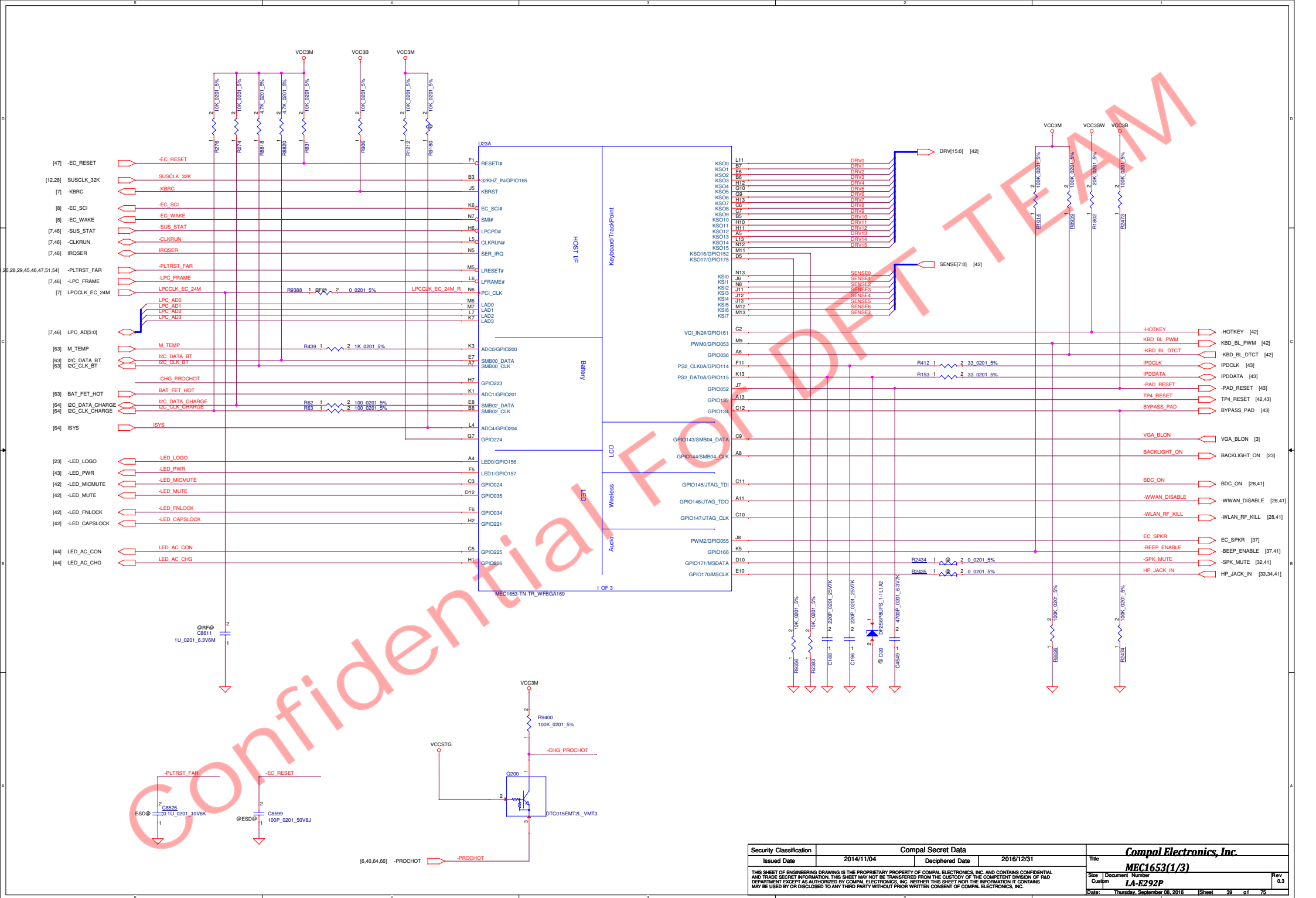
ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

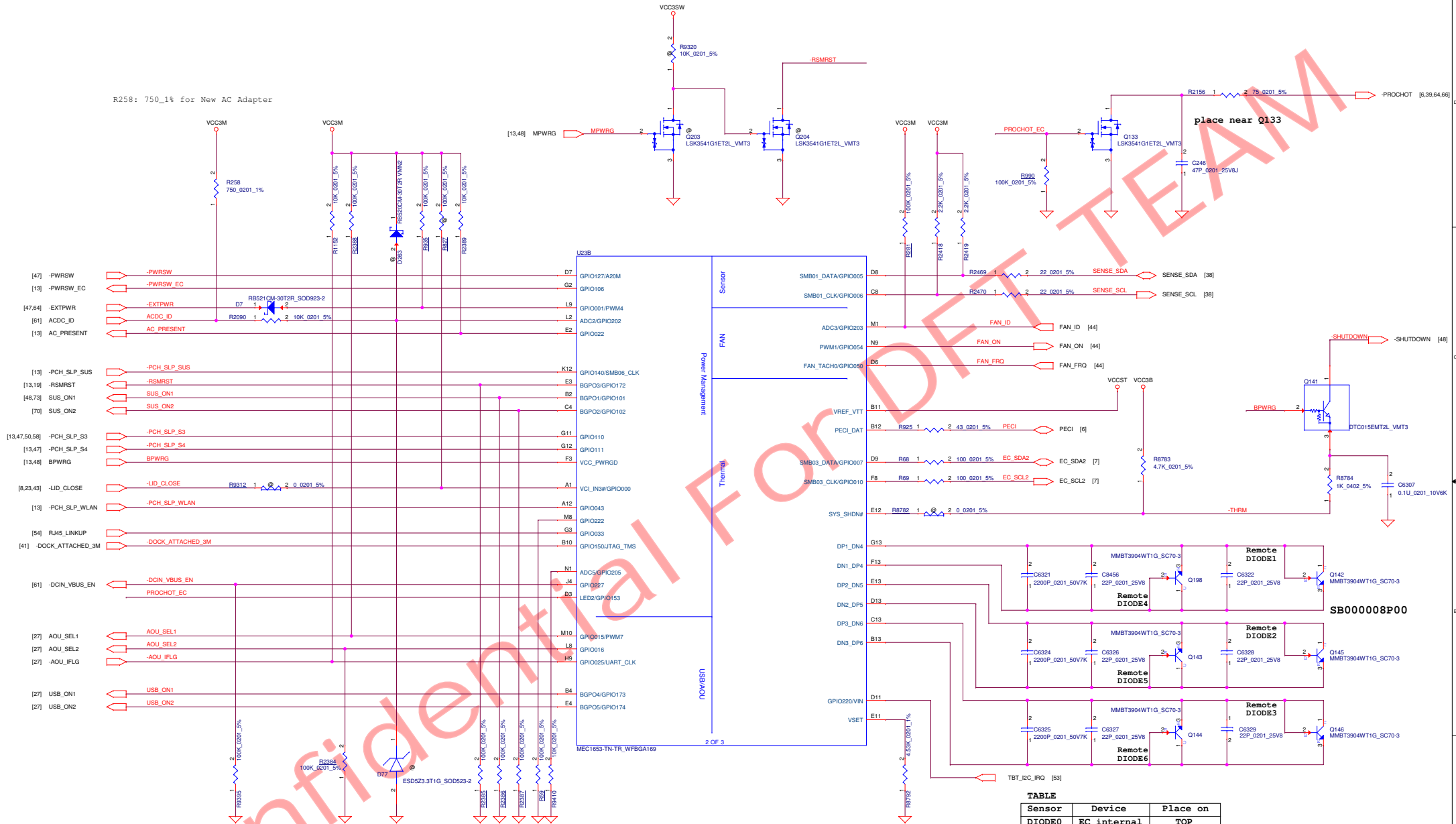


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R258: 750_1% for New AC Adapter

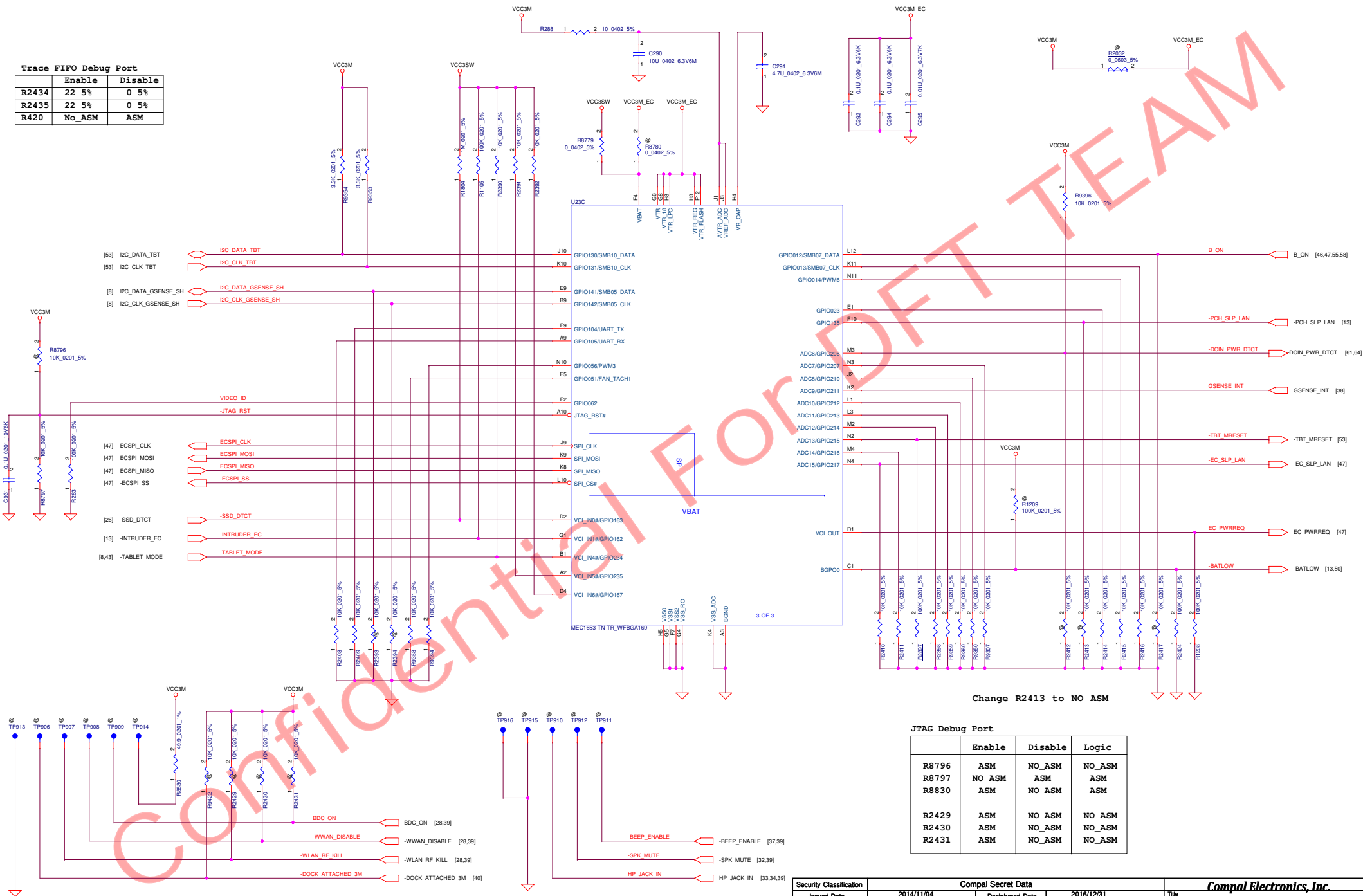


TABLE

Sensor	Device	Place on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	SSD	BOTTOM
DIODE3	DIMM	BOTTOM
DIODE4	FAN/HEATPIPE	BOTTOM
DIODE5	WLAN/WWAN	BOTTOM
DIODE6	CHARGER	BOTTOM

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Trace FIFO Debug Port		
	Enable	Disable
R2434	22.5%	0.5%
R2435	22.5%	0.5%
R420	No_ASM	ASM

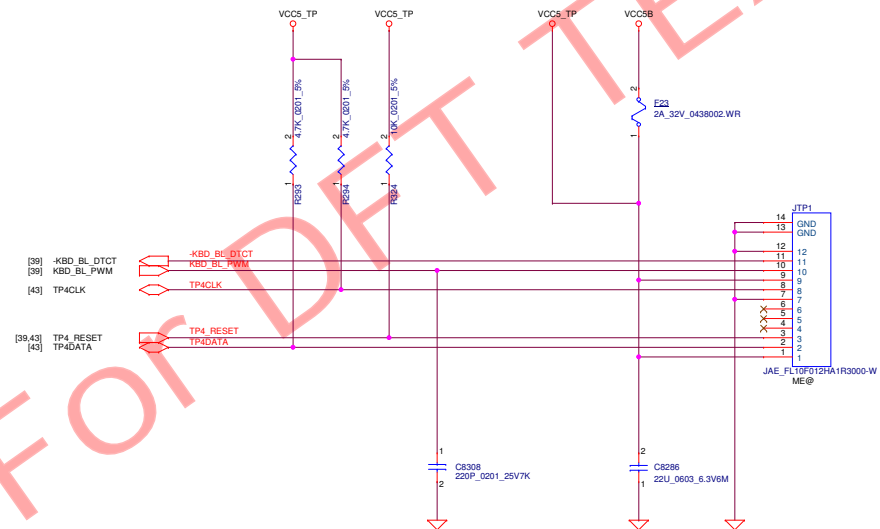
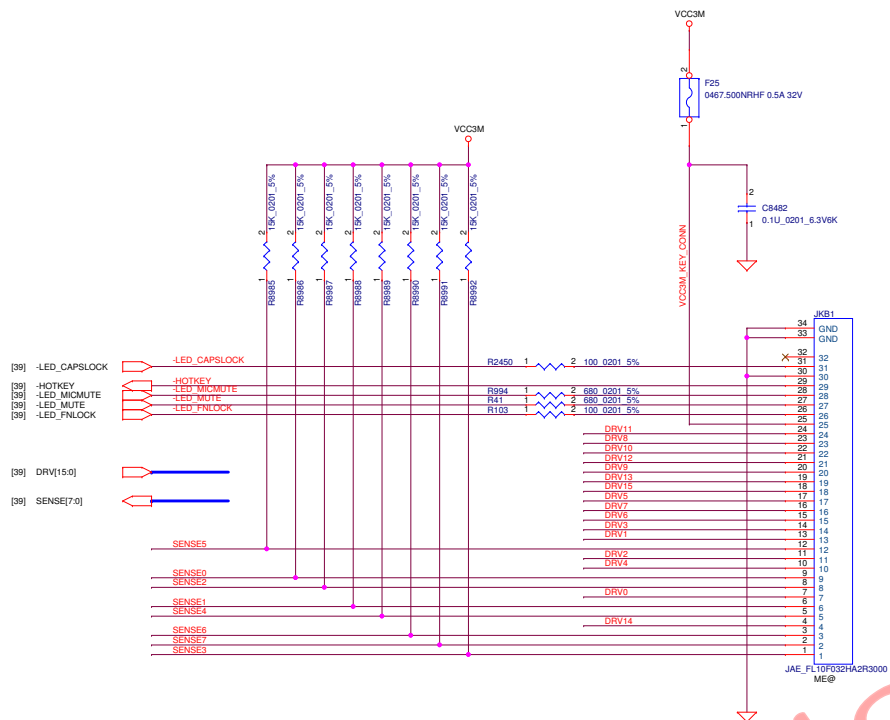


Change R2413 to NO_ASM

JTAG Debug Port

	Enable	Disable	Logic
R8796	ASM	NO_ASM	NO_ASM
R8797	NO_ASM	ASM	ASM
R8830	ASM	NO_ASM	ASM
R2429	ASM	NO_ASM	NO_ASM
R2430	ASM	NO_ASM	NO_ASM
R2431	ASM	NO_ASM	NO_ASM

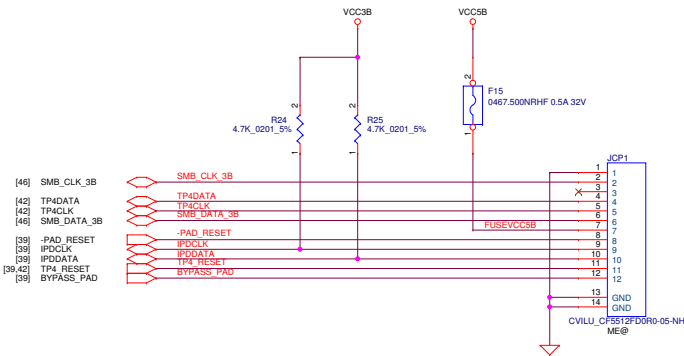
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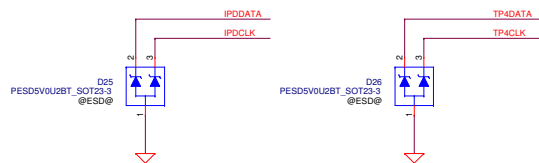
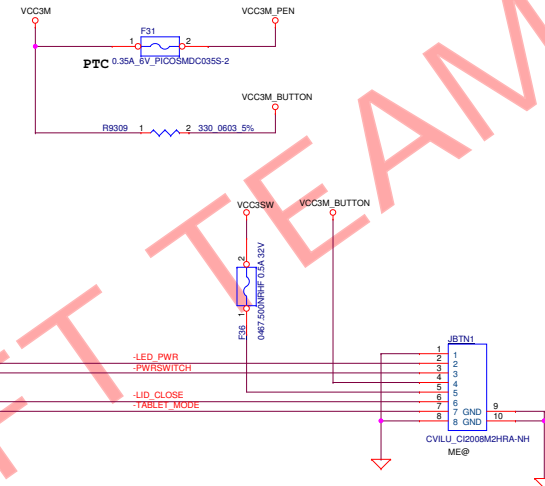
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Size		Document Number		Rev	
Custom		LA-E292P		0.3	
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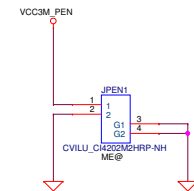
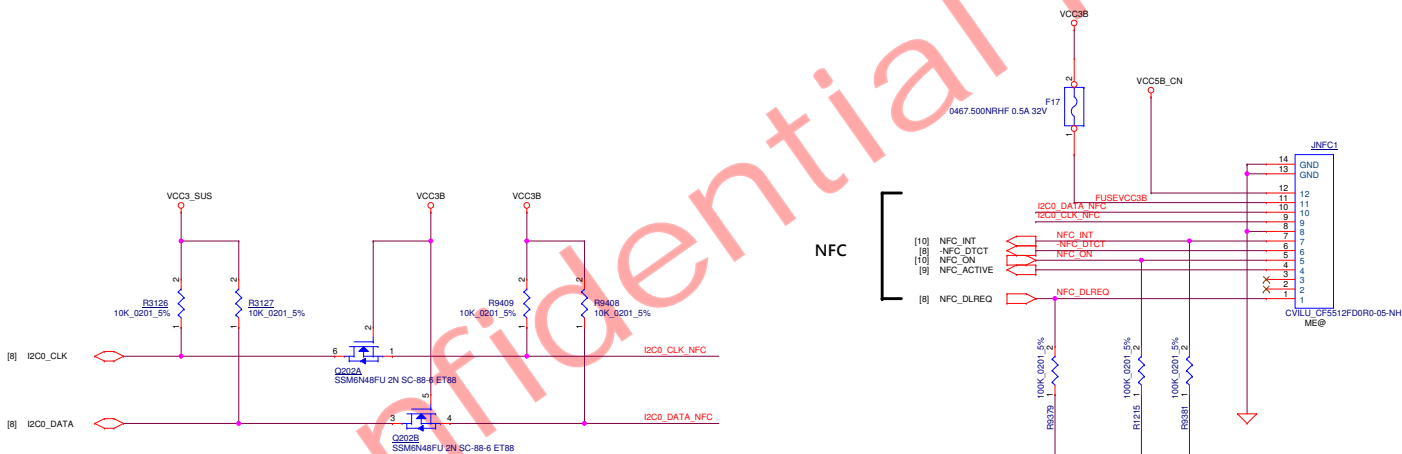
Clickpad



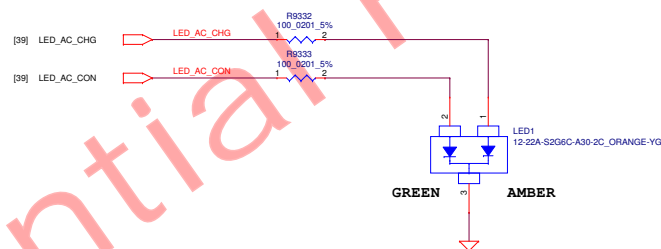
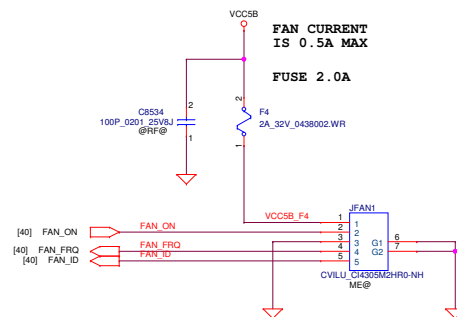
TO SUB BOARD



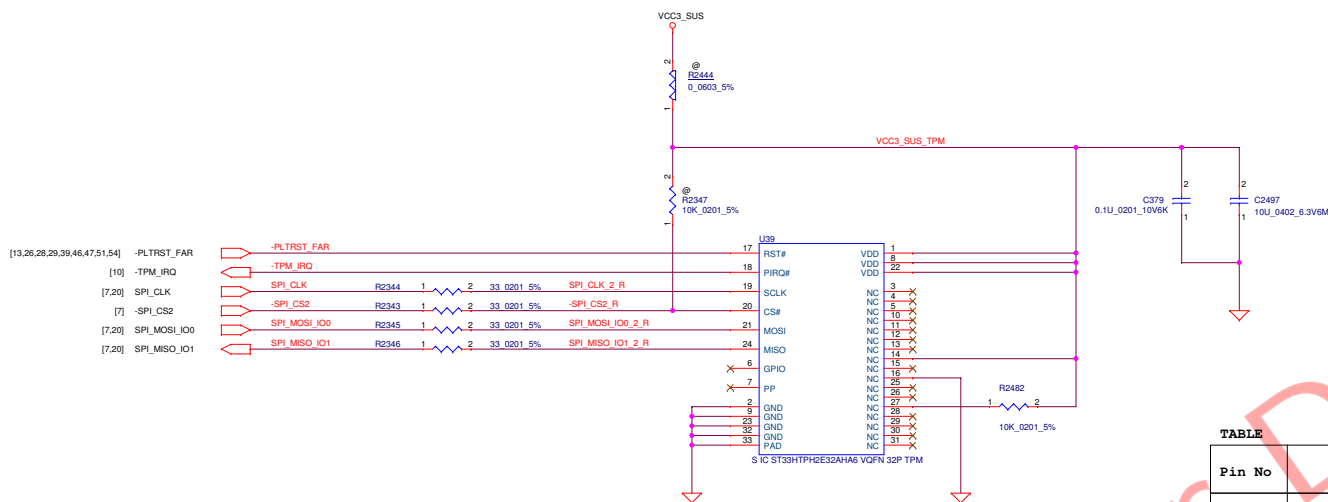
NFC



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				Custom LA-E292P
				Date: Thursday, September 08, 2016 Sheet 44 of 75



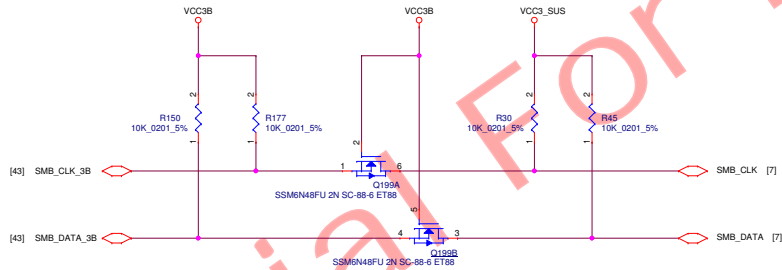
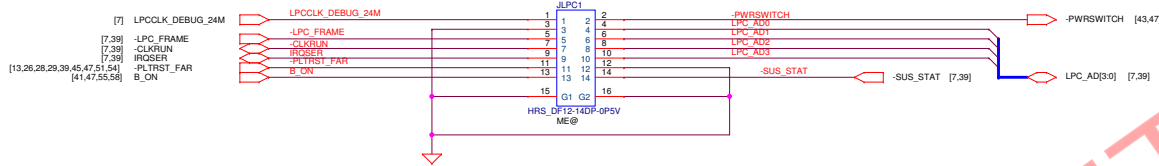
-Change TPM1.2 to TPM2.0
-Infineon SLB9670VQ2.0 part number SA00009N210
-ST ST33HTPH2E32AHA6 part number SA00009S010

TABLE

Pin No	ST ST33HTPH2E32AHA6	Infineon SLB9670VQ2.0 FW7.60
1	NC	VDD
2	GND	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	GPIO
7	PP	PP
8	NC	VDD
9	NC	GND
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	VDD
15	NC	NC
16	NC	GND
17	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK
20	SPI_CS#	CS#
21	MOSI	MOSI
22	VDD	VDD
23	NC	GND
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	GND

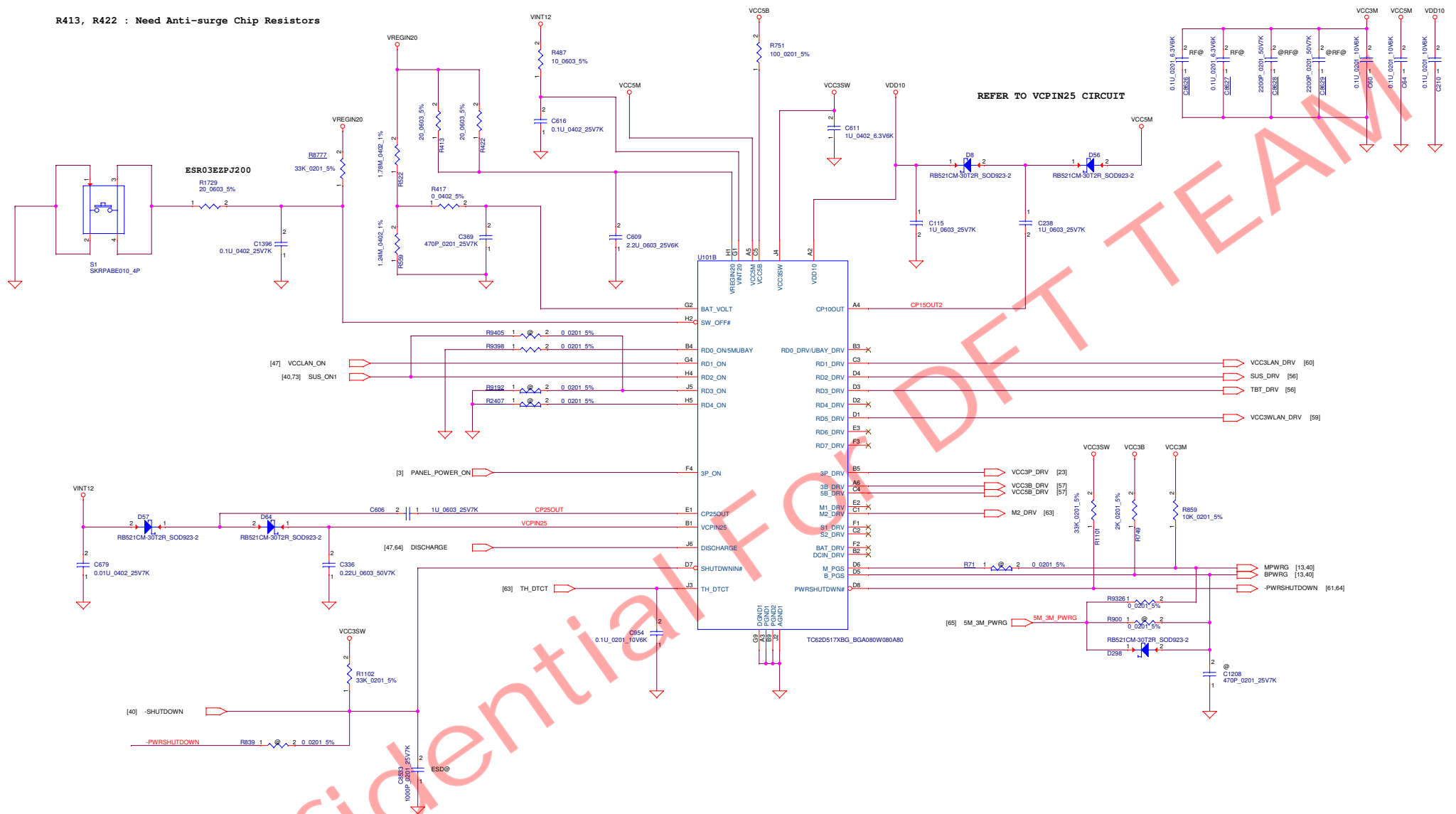
TABLE			
REF	DES	ENABLE	DISABLE
JLPC1		ASM	NO_ASM
R220		ASM	NO_ASM

↑
LOGIC



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2014/11/04		2016/12/31		SMBUS SWITCH/LPC DEBUG POR	
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		Custom		LA-E292P	
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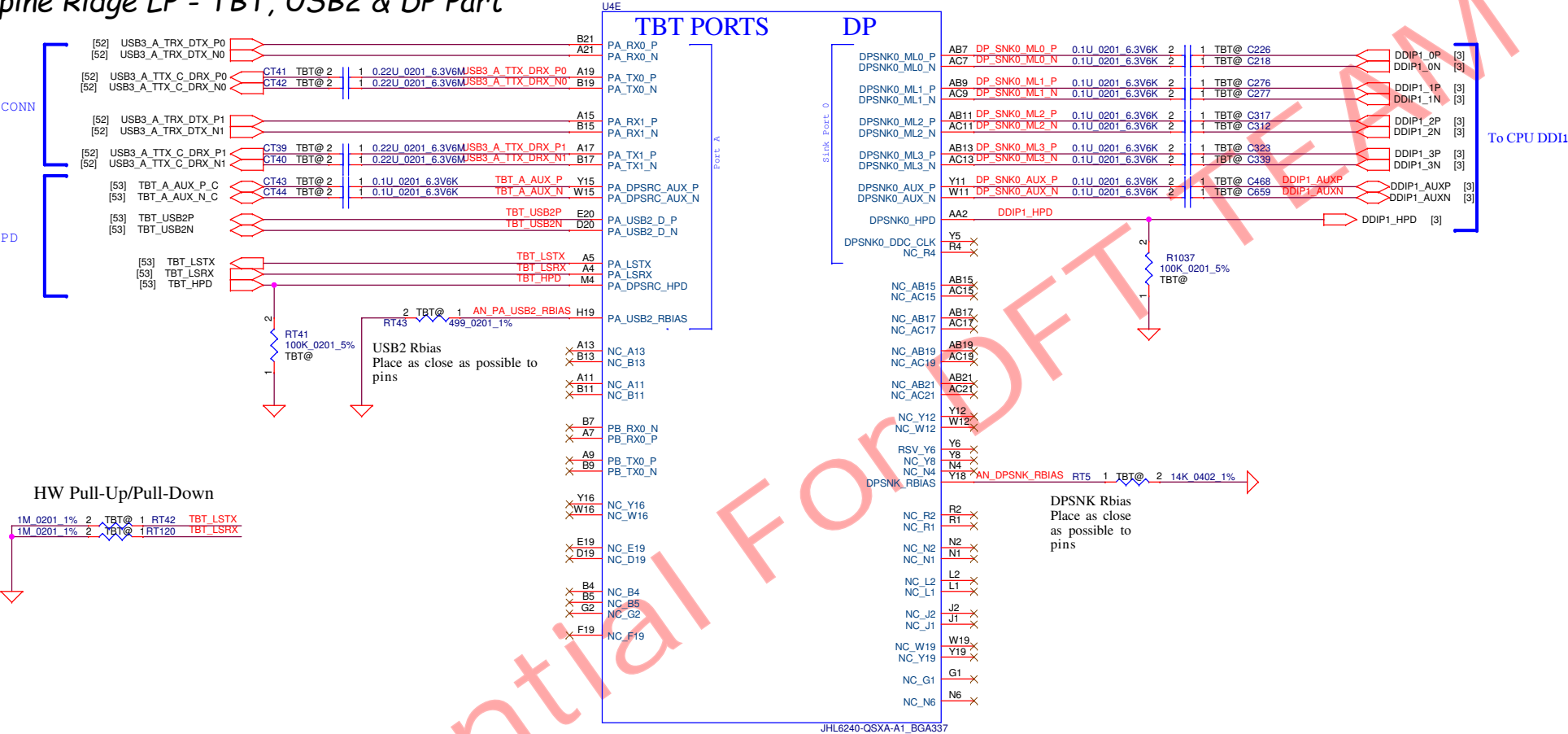
R413, R422 : Need Anti-surge Chip Resistors



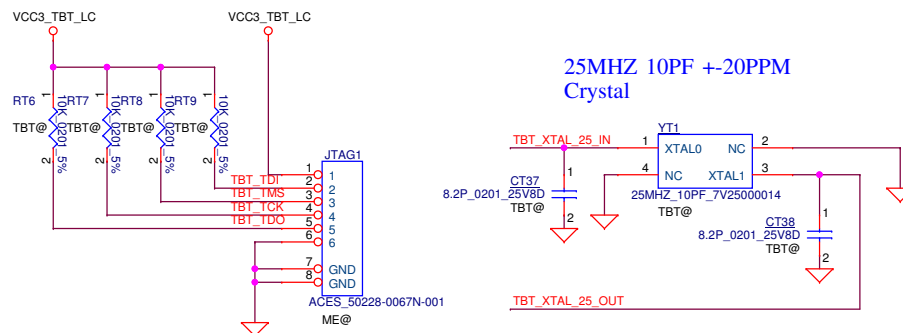
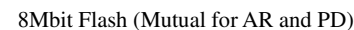
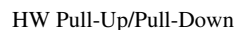
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	THINK ENGINE(2/2)		
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Alpine Ridge LP - TBT, USB2 & DP Part

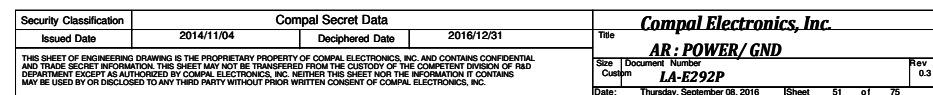
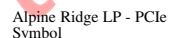
Alpine Ridge LP - TBT, USB2 & DP Part

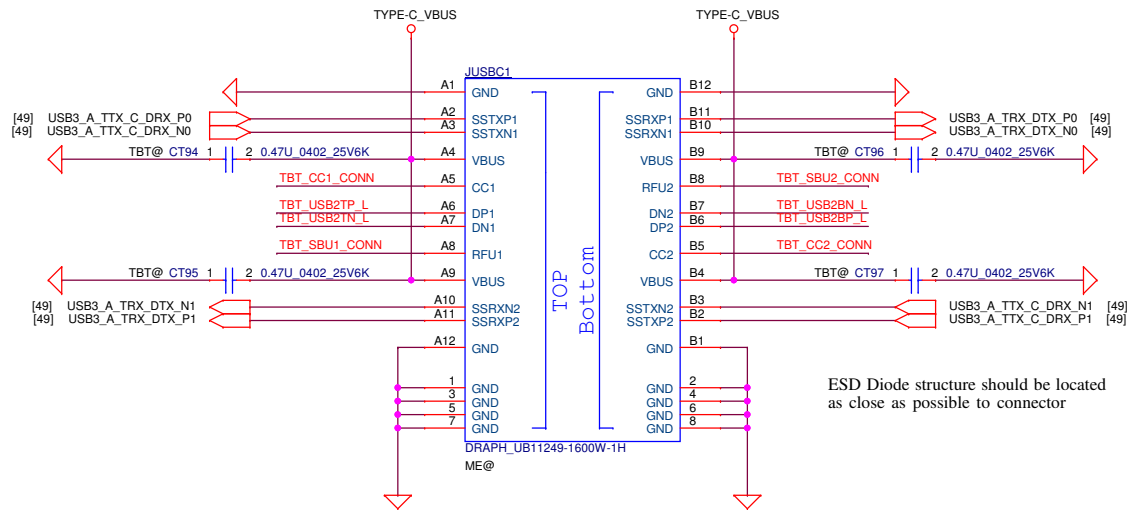


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Size A3	Document Number LA-E292P	Rev 0.3		Date: Thursday, September 08, 2016	Sheet 49 of 75

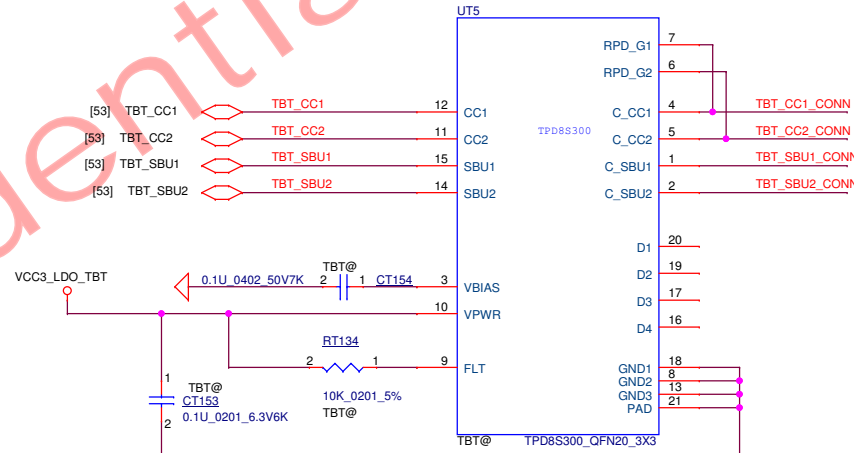
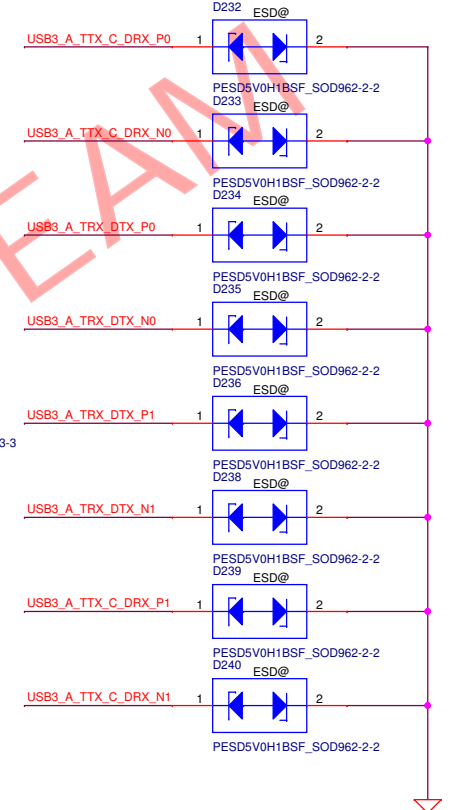
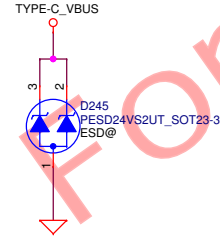
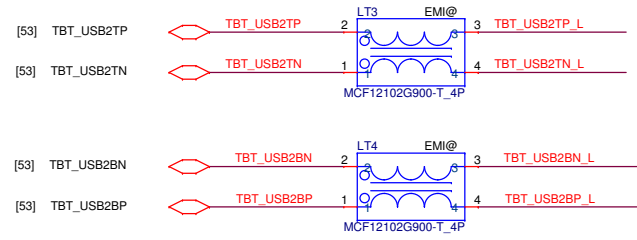
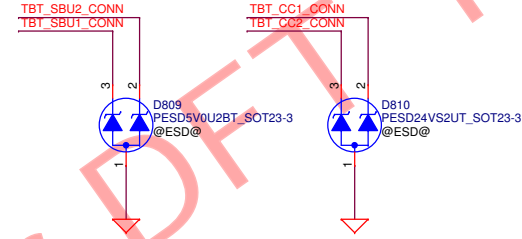
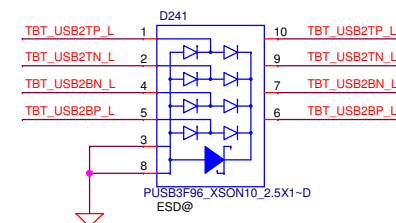
Alpine Ridge LP - Misc
Symbol

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Alpine Ridge SP - VCC
Symbol



ESD for USB2 Lines and Control lines



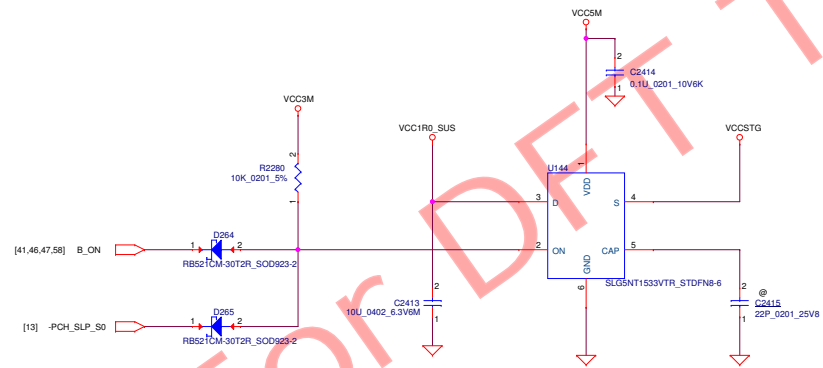
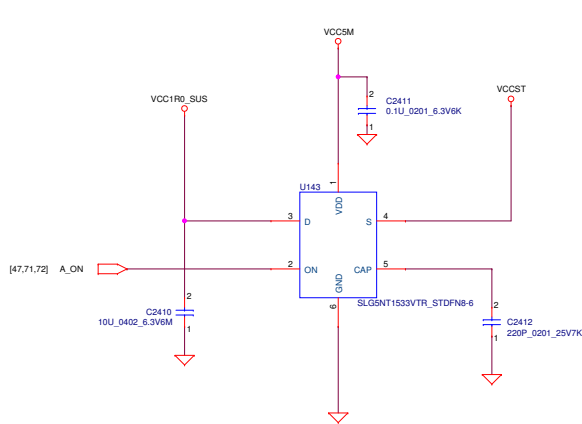
TBT_CC1 RT9354 1 @TBT@ 2 0.0201 5% TBT_CC1_CONN

TBT_CC2 RT9355 1 @TBT@ 2 0.0201 5% TBT_CC2_CONN

TBT_SBU1 RT9356 1 @TBT@ 2 0.0201 5% TBT_SBU1_CONN

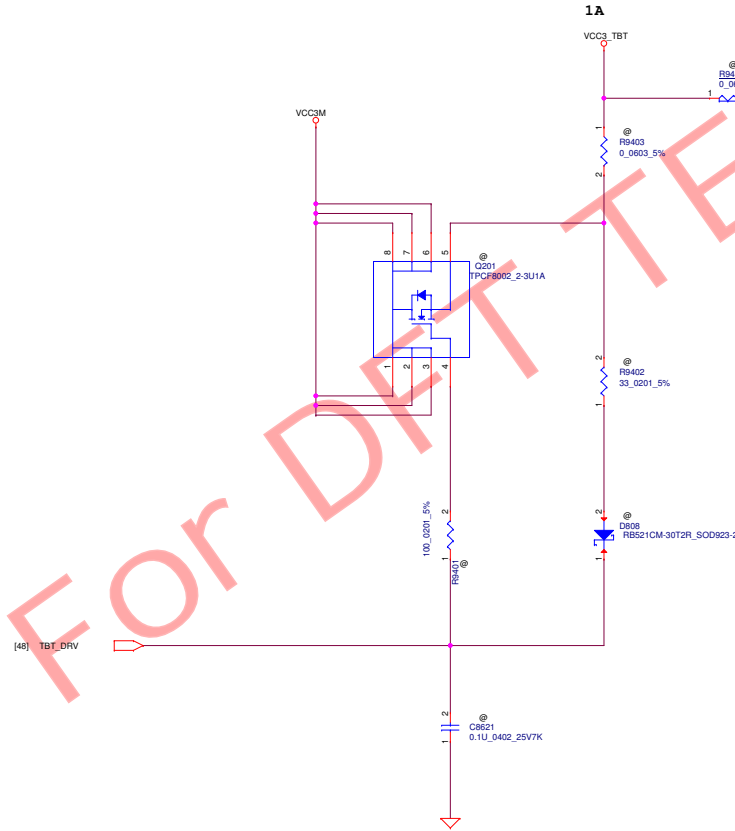
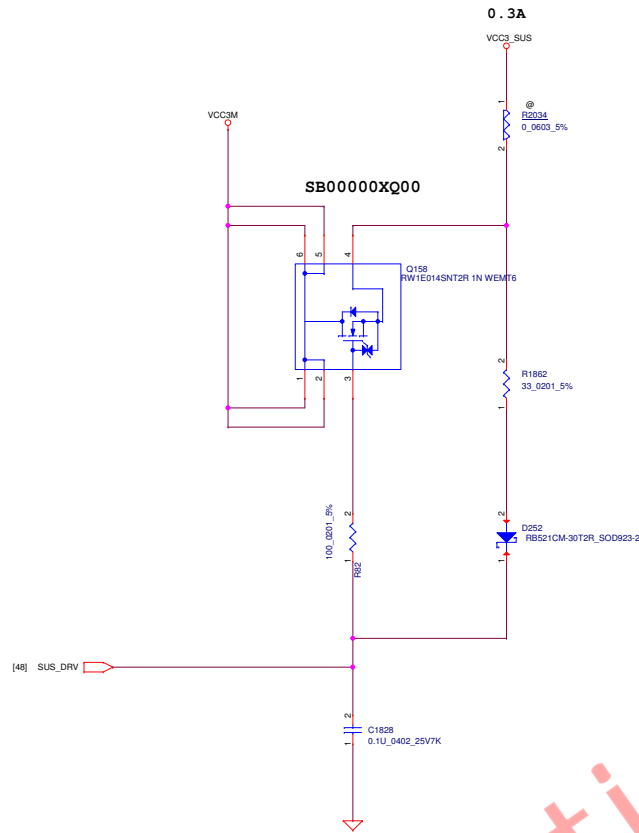
TBT_SBU2 RT9357 1 @TBT@ 2 0.0201 5% TBT_SBU2_CONN

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				Date: Thursday, September 08, 2016	Sheet 52 of 75

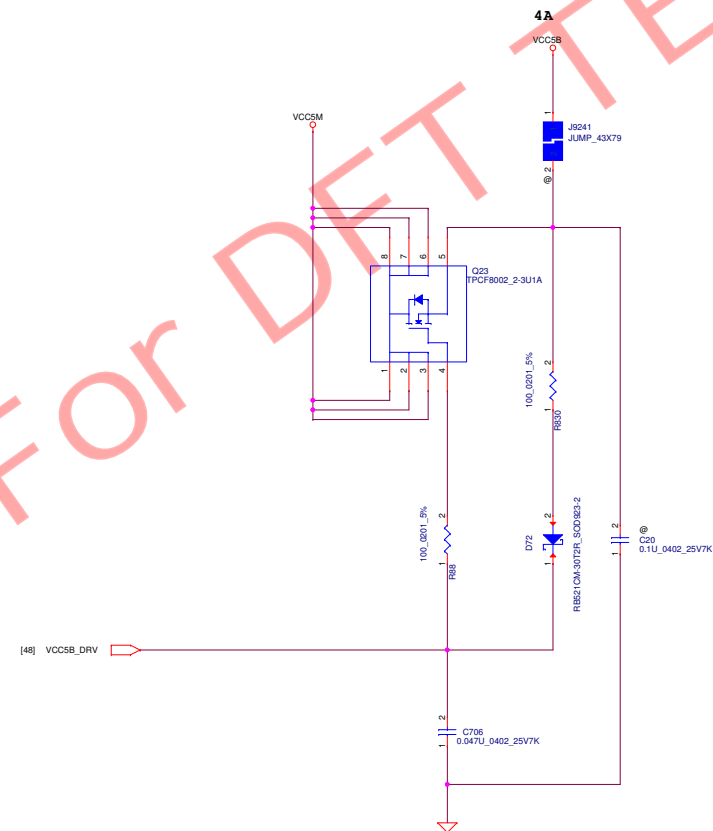


Confidential For DEFT TEAM

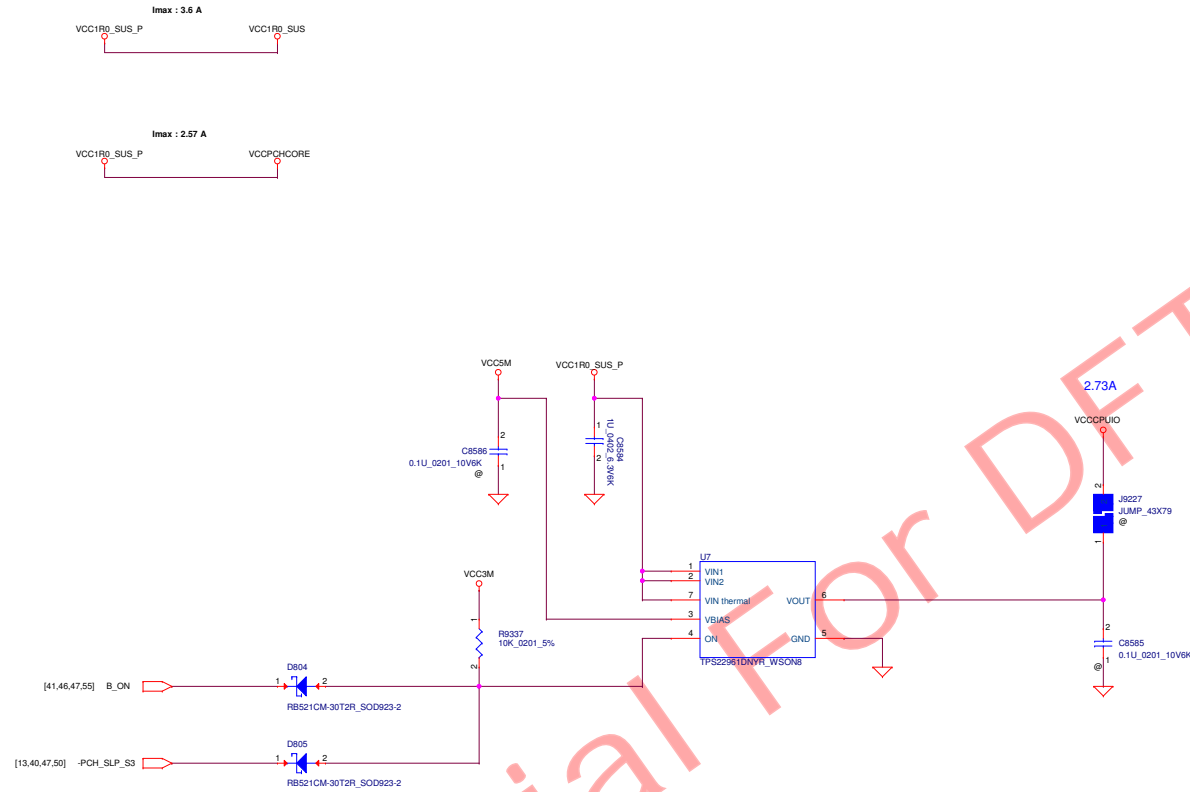
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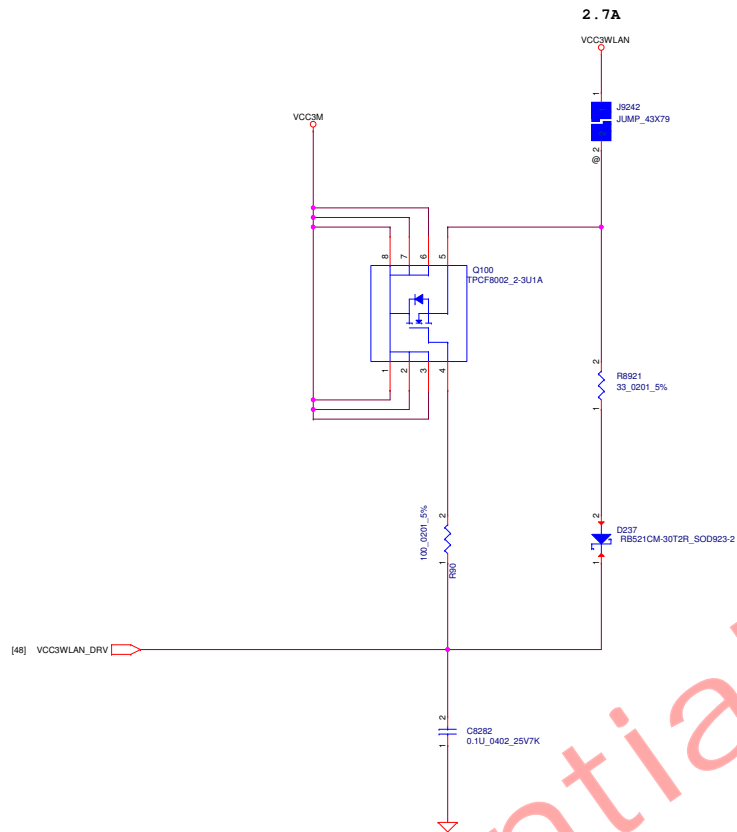
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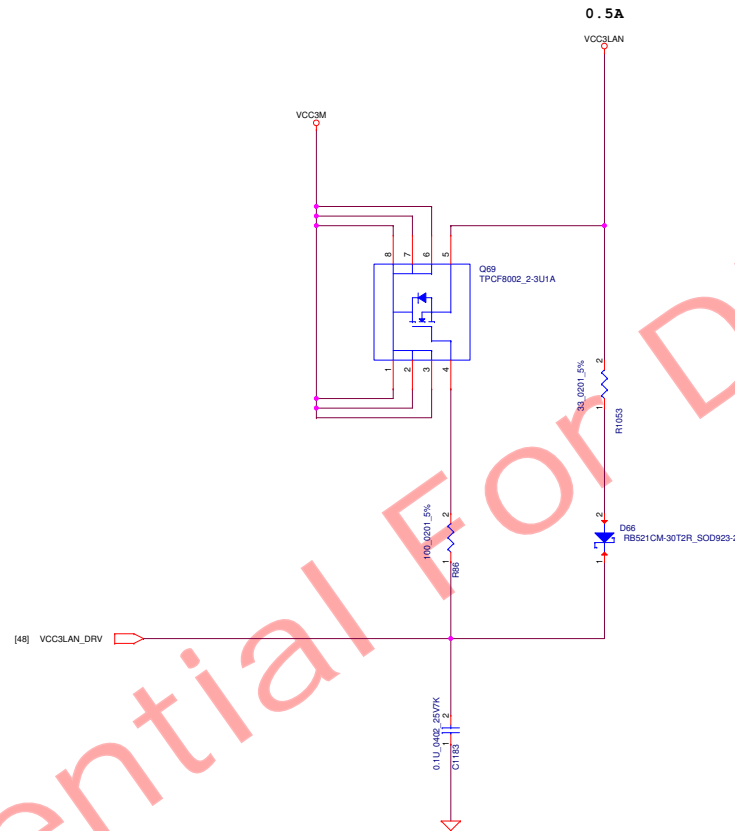
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	LOAD SW VCCCPU0
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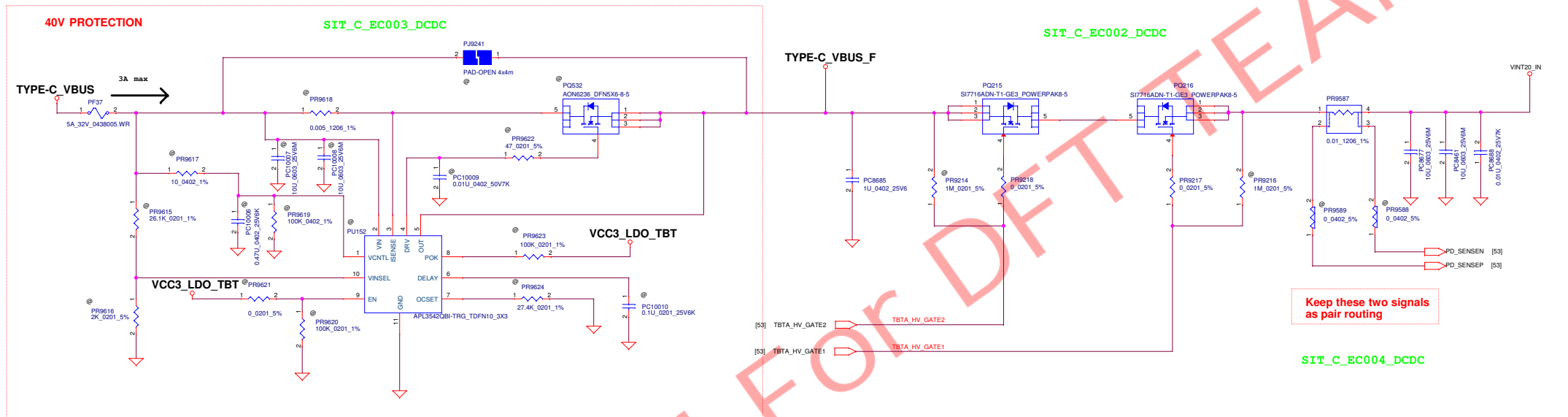
Confidential For DFT TEAM

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				Document Number	0.3
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Confidential For DFT TEAM

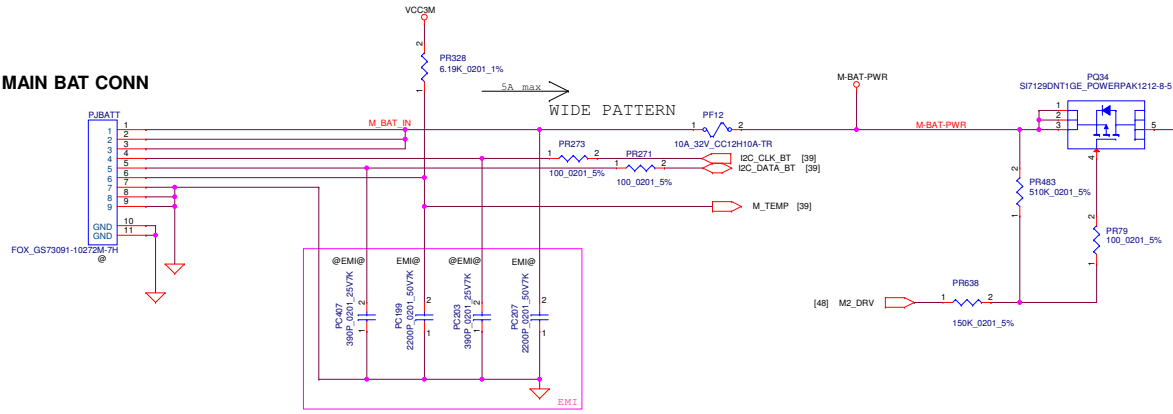


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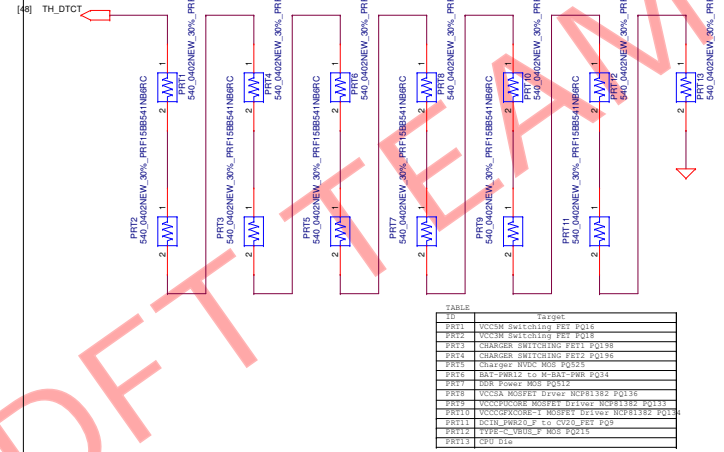


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MAIN BAT CONN

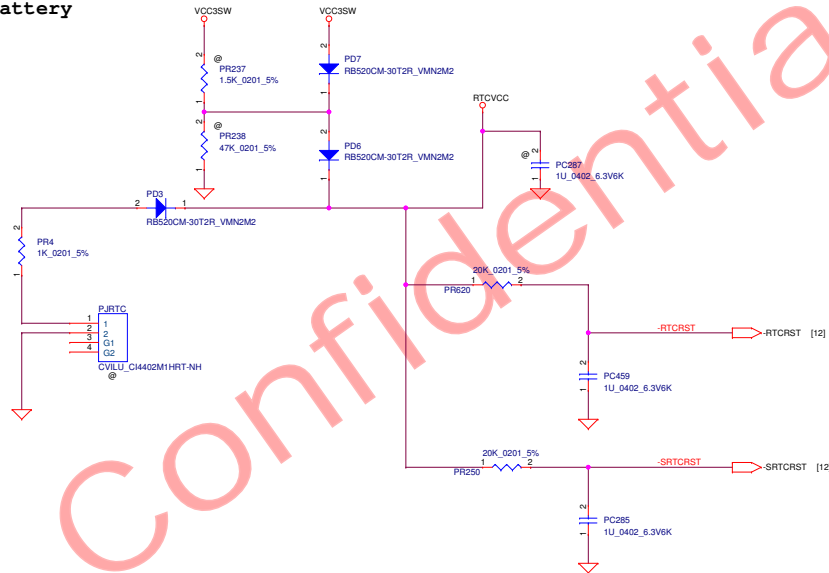


PTC function



Target	Target
PT1	VCC3M switching FET P019
PT2	VCC3M switching FET P019
PT3	CHARGER SWITCHING FET1 P019
PT4	CHARGER SWITCHING FET2 P019
PT5	CHARGER SWIC- MOS P025
PT6	BAT-PWR12 to M-BAT-PWR P034
PT7	BAT-PWR12 MOS P034
PT8	VCC3M MOSFET driver NCF1382 P0136
PT9	VCC3M MOSFET driver NCF1382 P0136
PT10	VCC3M MOSFET driver NCF1382 P0136
PT11	DCIN_PWR20_F to CV20_FET P03
PT12	DCIN_PWR20_F MOS P015
PT13	CPU Dis

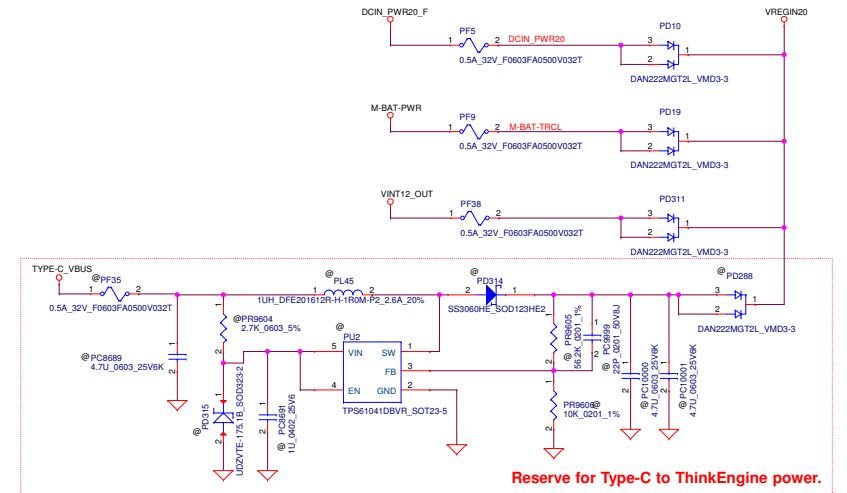
RTC Battery



FVT_EC002_DCDC

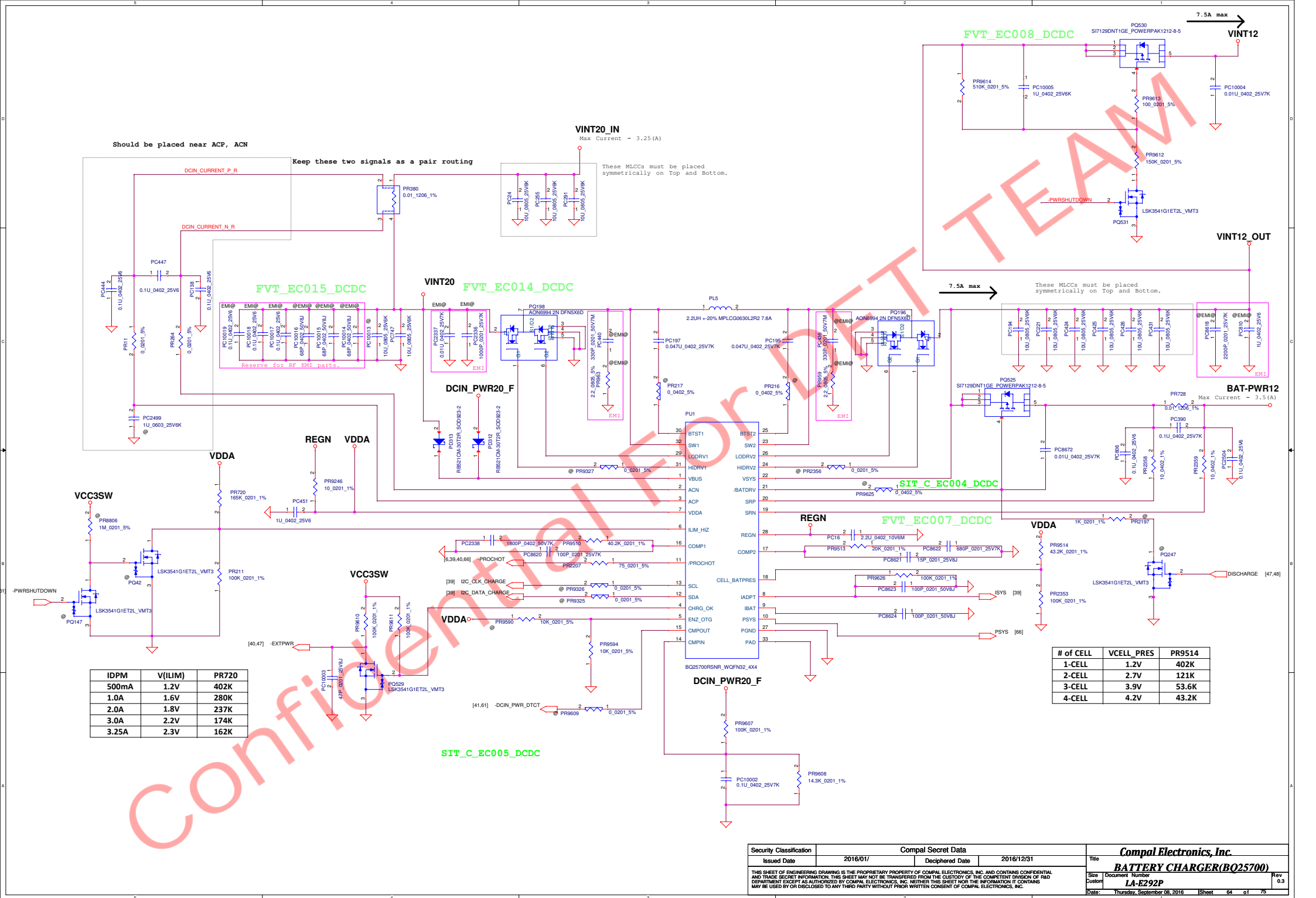
FVT_EC003_DCDC

Power to ThinkEngine



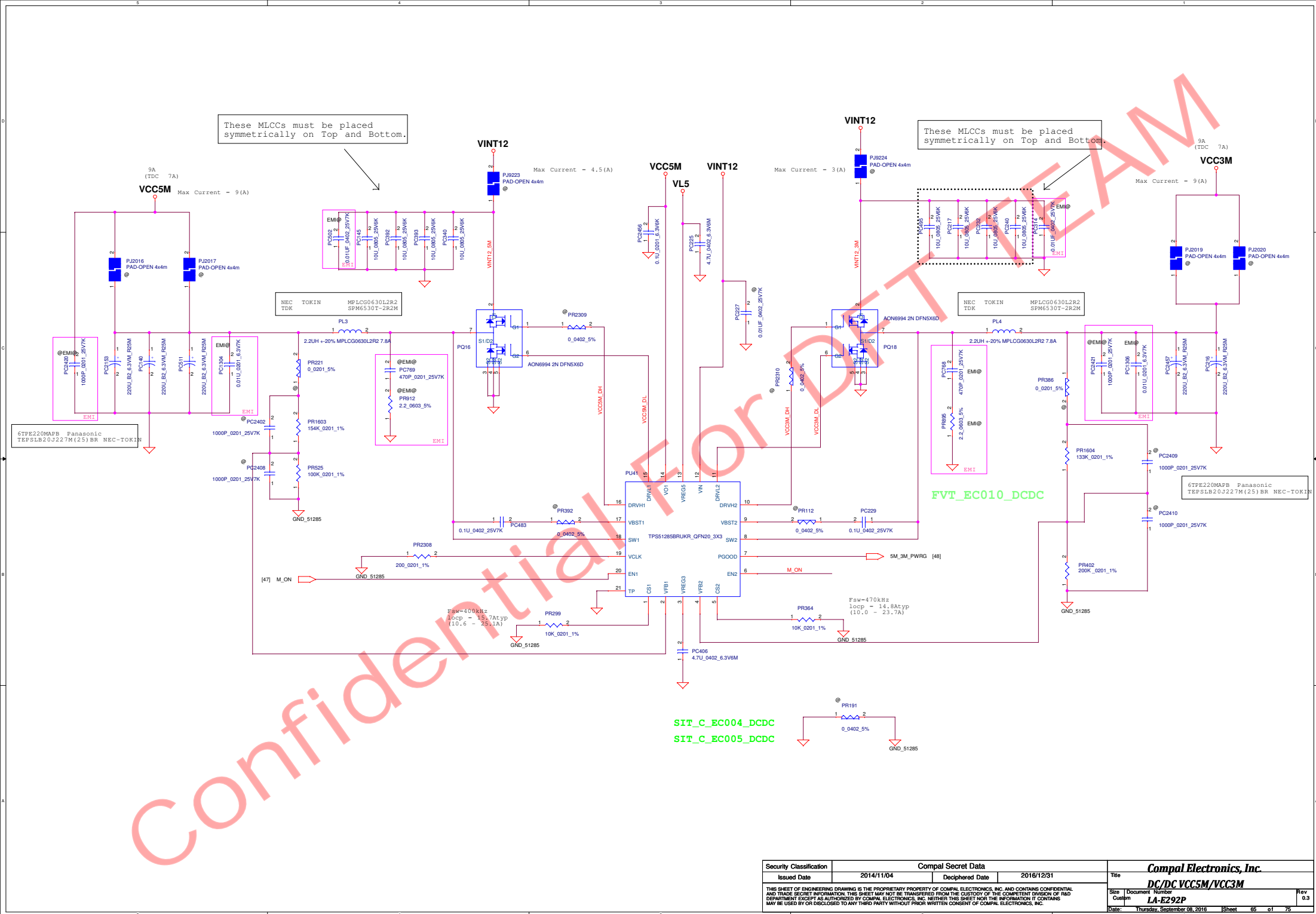
Reserve for Type-C to ThinkEngine power.

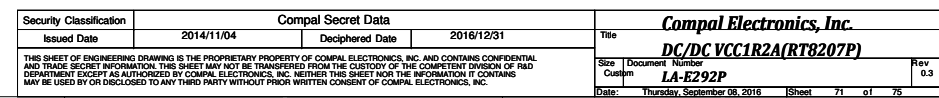
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Size	Document Number	Rev	0.3
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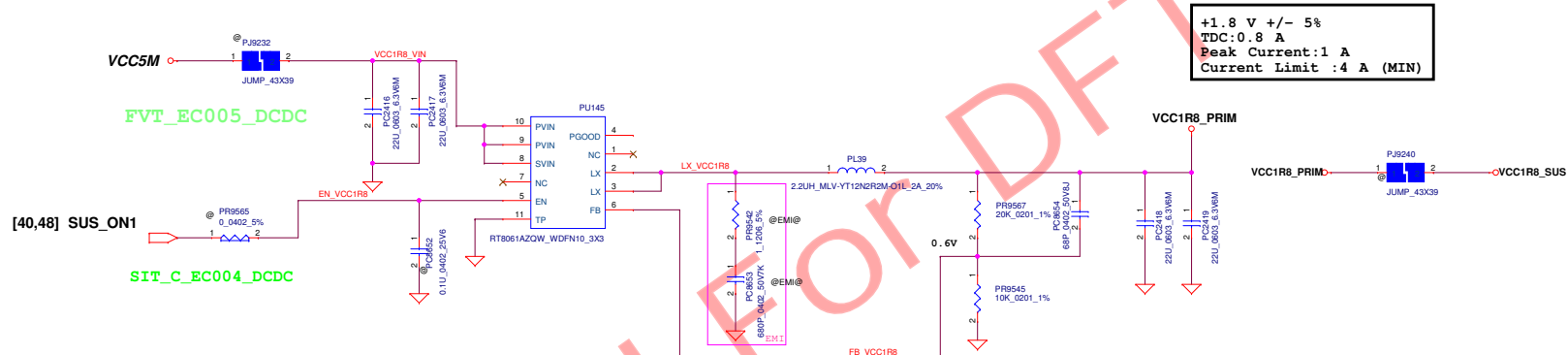


IDPM	V(ILIM)	PR720
500mA	1.2V	402K
1.0A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

# of CELL	VCELL_PRES	PR9514
1-CELL	1.2V	402K
2-CELL	2.7V	121K
3-CELL	3.9V	53.6K
4-CELL	4.2V	43.2K





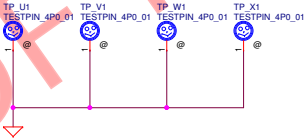
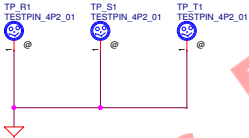
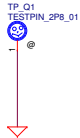
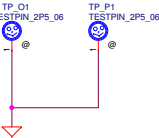
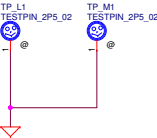
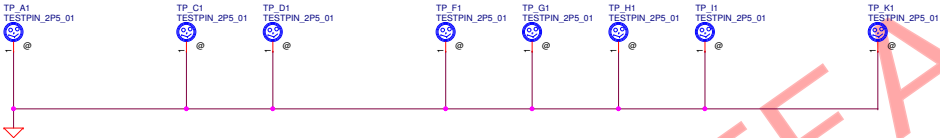


+1.8 V +/- 5%
TDC: 0.8 A
Peak Current: 1 A
Current Limit : 4 A (MIN)

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PTH FOR SCREW HOLE

Value	Hole Dia	Pad Dia		QTY
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	9
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



TP_Y1
H_2P5N
H_2P5N

TP_E1
H_4P0X2P5N
@H_4P0X2P5N

FID
Board Area

FD1
NC, NO CONNECT TO ANY.

FD4
NC, NO CONNECT TO ANY.

FD2
NC, NO CONNECT TO ANY.

FD3
NC, NO CONNECT TO ANY.

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title
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Date: Thursday, September 08, 2016				Rev 0.3
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ZZZ
DAB001BL000
DIMM

ZZZ1
DAB001BM000
On board

U58
KBL OKKS 2.4G
CPU1#
SA00009PJ40

U58
KBL OKJW 2.6G
CPU2#
SA00009JUR20

U58
KBL OKDP 2.4G
CPU3#
SA0000A3840

U58
KBL OKDN 2.7G
CPU4#
SA0000A3410

U58
KBL OKDM 2.5G
CPU5#
SA0000A3740

U58
KBL OKDU 2.6G
CPU6#
SA0000A3L00

U58
KBL OLYG 2.6G
CPU7#
SA0000AD000

U58
KBL OLYF 2.8G
CPU8#
SA0000ADP00

U13
Jacksonville WGI219V
NVPRO@
SA00009S410

ZZZ
Samsung 1G
S1G@
X7666239L24

ZZZ
Micron 1G
M1G@
X7666239L22

ZZZ
Samsung 2G
S2G@
X7666239L23

BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO LAN chip	VPRO@	WGI219LM
non vPRO LAN chip	NVPRO@	WGI219V
Thunderbolt requirement	TBT@	
Thunderbolt reserve	@TBT@	
ESD requirement	ESD@	
ESD reserve	@ESD@	
EMI requirement	EMI@	
EMI reserve	@EMI@	
RF requirement	RF@	
RF reserve	@RF@	
XDP	XDP@	
On board RAM	X76@	